Contact Chains for FinFET Technology Characterization

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***Abstract*—Electrical characterization remains a key element in technology development and manufacturing of integrated circuits. Contact chain is a well known part of the diagnostic set of test structures used across many generations of silicon processes. Implementation of such test structures becomes challenging in new technologies with 3-D devices, like FinFET. Contacts to active regions of such devices are inherently dependent on the architecture of epitaxial raised source and drain and for proper characterization require the presence of transistor gates, which set the environment for contacts. This paper describes a new type of test structure, so-called gated contact chains, developed for contact process characterization in FinFET technologies. Instead of simple chain of contacts, each structure contains a series of active devices with common gate electrode used to turn on the chain of transistors to enable measurement of chain resistance. To discriminate between chain failures caused by an open contact or by other mechanisms (e.g., bad transistor with very high threshold voltage) a series of measurement under various test conditions was performed and analysed. In order to overcome a limitation of the contact chain size and enable data collection from larger sample of contacts, we proposed to implement the gated chains in addressable arrays, increasing their density and failure rate observability. Finally, the paper presents the examples of electrical failure modes detected by those chains in FinFET process.**

***Index Terms*—FinFET, CMOS, characterization, contacts, test structures, failure mode.**

I. Introduction

PROCESS characterization and diagnostics are vital elements of semiconductor manufacturing, first in technology development, and later in process control in mass production. It is done in various ways, with metrology, inspection, or electrical test. Various test structures are designed to collect information about the process, modules, and devices. Some are very simple, and provide assessment of one parameter, exploring its dependence on several geometrical and process-related factors, others are complex, and the measured output is a combination of multiple parameters and/or failure modes.

Contact chain test structure has been used for diagnostics for many years [1], [2]. It is a well established tool – it is simple to design and easy to perform electrical measurements.

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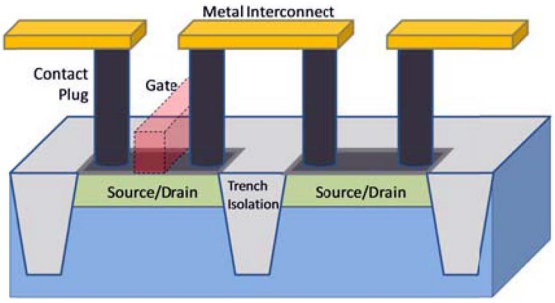

Fig. 1. Contact chain schematics for "traditional" planar MOS technology.

Its application spans from technology development to process monitoring in manufacturing, where it can be used to detect contact failures across multiple design attributes (substrate type, space, density, active enclosure, etc.). Traditionally, the test structure is designed as a passive chain of contact links with lower connectors (Silicided Active or Poly-Silicon stripes) and upper connectors (typically Metal line segments), as shown in Fig. 1. Although in a real device the contacted regions would be separated by a transistor gate, the presence of the gate in the test structure is usually not necessary, as it has rather limited impact on contact behavior or failure mechanism. In traditional CMOS technologies contact chains with no gate have been representative for a typical contact, and failure modes of such chains represented failure mechanisms observed in functional logic or memory blocks.

However, advanced silicon technologies, especially the technologies which use the Replacement Gate (Gate Last) integration schemes [2], are much more challenging. Metal gate and epitaxial Source and Drain create unique topographical conditions, which define contact height and shape. Fin silicidation, performed locally inside the contact hole determines contact resistivity, as well as sensitivity to potential failure modes. In such situations, process characterization requires that the test structure replicates the contact environment which is present in real devices built with fully integrated process flow. This unique sensitivity and the need to characterize the contacts in true transistor setting has been also recognized in recent publications [3], [4].

A. Contacts in FinFET Devices

Recent developments in advanced technologies introduced a new device architecture and 3D integration – FinFET [5],

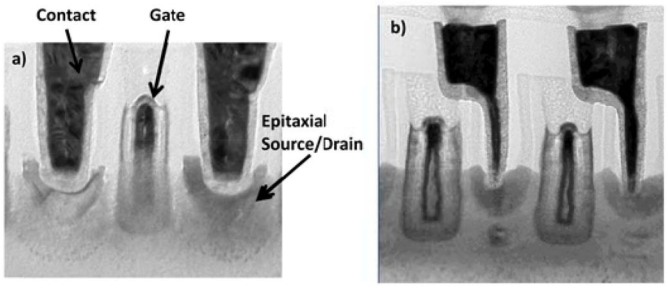

Fig. 2. Source/drain contacts in FinFET transistors (after [8]). Raised epitaxial source/drain region overgrowth determines the contact quality (a); and contact-gate alignment impacts resistance and risk of failure (b).

with new failure modes and characterization challenges. Since device contact regions are created by selective epitaxy as raised Source/Drain grown on Fins [6], [7], the contact chain built as a set of passive contacts with lower and upper runners is not representative any more. In true FinFET-based circuits, contact characteristics are defined by the Contact W plug geometry, as well as the shape, size, doping, and silicide of the contacted active regions. Fig. 2 shows examples of FinFET contacts from 22nm node technology [8].

Full characterization of failures in such technology needs to account for two issues:

- The volume and the height of raised Source/Drain grown on the Fins depends on the presence of the Gates; the Contact Open failure rates would be different if the Contact lands on a Fin without Gate neighborhood
- Sensitivity to misalignment of the Contact to the Gate – the Contact size, and consequently its failure rate is determined by the presence of the Gate and Gate-Contact interaction [as shown in Fig. 2(b)].

As a consequence, the contact chain which really needs to be characterized is shown in Fig. 3(a). It contains not only simple contact plugs with lower and upper runners, but the whole transistor element, with junction topology and contact configuration. Fig. 3(b) and (c) show the Active regions as segments of Fins, and how the Gate presence impacts the "gate-bound" epitaxial growth of raised Source/Drain regions.

The test structure built only out of active region Fins, contacts, and interconnect runners, and with no Gate patterns, would suffer from very poor Epitaxial Si/SiGe growth, and would not represent true shape and height of the contacted region. Epitaxial process used for growing raised Source/Drain on Fins has a very strong sensitivity to design and layout details [9]. Gate/STI neighborhood, Fin size, and density of patterns impact growth rate, faceting, and stress. Consequently, the traditional contact chain structure would provide rather limited value as a characterization tool in process development or process monitor in manufacturing. The results collected from such structures would be questionable, as additional failure modes, not present in real process could dominate the test results.

B. Characterization Requirements

To meet the above requirements, the test structure needs to include the Gate elements, and in consequence the chain

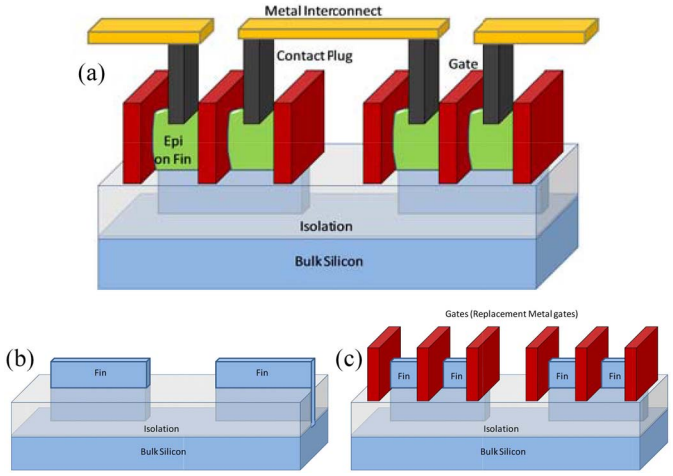

Fig. 3. Contact chain schematics for 3D FinFET technology (a). Illustrations (b) and (c) show construction elements of FinFET integration required to replicate contact environment.

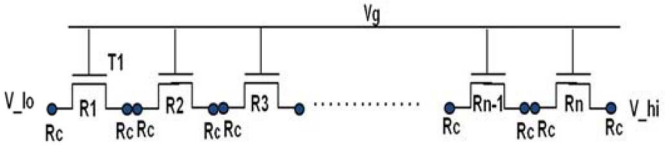

Fig. 4. Schematic diagram of contact chain with transistor "links." Transistors gates are connected to common terminal and sufficiently large gate voltage Vg (Vg >>Vt) is applied during test to enable measurement of the chain resistance.

becomes a series of device segments, as shown in Fig. 3(a). This transistor chain can be tested in 3- or 4-terminal configuration, similar to a single transistor. Gate terminal would be used as a common gate to turn ON all devices in the chain. Test and analysis of such chains (called here Gated Contact Chains) present a significant challenge, since unlike a passive chain, the Gated chain resistance is a strong function of test conditions and device properties, especially Fin resistance and the threshold voltage Vt of the devices. The problem becomes especially important in early technology development, when Vt may not be stable and vary greatly from wafer-to-wafer, across the wafer, and across process split conditions.

II. Test Structure Design

As discussed above, process module integration puts special requirements on the design of the chains. To address this need we proposed a new test structure - Gated Contact Chain. Fig. 4 shows the schematic of this structure - 4-terminal chain of transistors with Low and High terminals, a Well terminal, and a common Gate shared by all devices.

Each device "link" contains two contacts and one intrinsic transistor, so the chain of N devices has 2N contacts. Obviously, the chain can contain any number of links. Different chain structures can have different design attributes (e.g., 1-Fin vs 2-Fin device, Short vs Long Gate, Wide vs Narrow Contact Bar, etc)

Each gated chain structure requires at least 3 terminals for testing - Low Pin, High Pin, and the Gate terminal.

In bulk technologies the Well contact can be tied up to the Low Pin or High Pin terminal during testing. If desired, the Well can be reversely biased with respect to Source/Drain to reduce background leakage of the junctions. In such case, a side effect of the back-bias on Vt of the devices in the chain needs to be taken into account when choosing the test conditions.

The Well terminal can also be used to assess Junction leakage of the structures with abnormally high output current I_hi (very high junction leakage can impact the resistance measured across the chain and give erroneous results).

A. Number of Structures in the Chain

The decision on what is the right number of contacts (and device links) in the chain is a rather challenging question, as there is a trade-off between detectability of a failure, and observability of the failure rate.

On one hand, we would like to have very high count of contacts in the chain to increase chances to catch and detect "bad" (open or high resistive) contact. Typical passive Contact Chains used for process monitoring often employ as many as tens of thousands contacts in one chain. This is hardly achievable with Gated Contact Chains.

On the other hand, we still want to preserve detectability of a failure, which requires that the electrical response (e.g., current) of a failing structure is distinctively different from that of a good structure. The resistance of the chain increases with the count of device "links", and the chain current decreases for the same V_hi and Vgate conditions Also, Vt variability adds to the chain current variability, and one has to account for this variability when setting the criteria to distinguish "Pass" from "Fail" contact chain.

In order to fulfill both requirements, we designed Gated Contact Chains with various contact counts, varying from 10-800. Obviously, the optimum number depends on the technology details, like contact resistance, device performance, Vt target and Vt variability, and so on.

Below we report the results collected on test structures with 200 device links, i.e., 400 contacts.

B. Test Organization for Increased Observability

One of the consequences of using a small contact chain is low observability of failure rates. It is difficult to capture a bad contact with small chains if the occurrence frequency of bad contacts (i.e., failure rate) is low. To increase observability, one has to replicate the test structure many times and collect the test data from all the replicates, ideally from all dies across the wafer (to realize highest observability and create realistic wafer maps of contact failures).

A downside consequence of having large number of test structures is the test time, which increases proportionally to the number of test structures. To address this problem we propose a twofold approach:

- The test is simplified and performed at a single test condition (V_hi and Vg), and based on the value of the measured current, structures are classified as "Pass" or "Fail". Failed structures can further be tested with more elaborate test to assess a failure mode (see Section III)
- The test can be performed in parallel on multiple structures within same die. There are multiple solutions and opportunities, briefly discussed in Section IV.

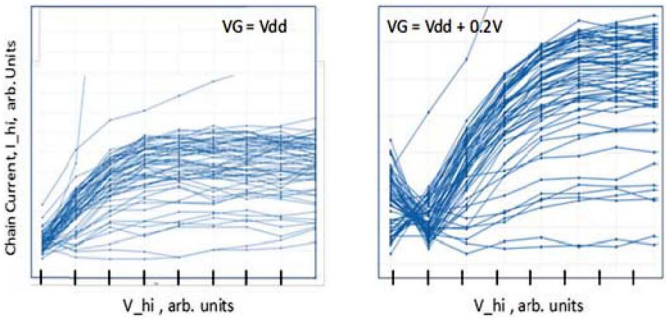

Fig. 5. I-V curve traces of gated contact chains collected from a FinFET wafer at two different gate voltage levels. With higher gate overdrive, high resistive chains start separating from the main distribution.

C. Test Conditions

One of the assumptions for testing Gated Contact Chains is that the resistance of the devices should be as low as possible, so that any element of the chain with high resistance can be easily identified as an outlier. This dictates usage of the gate voltage as high as possible, to make sure that all devices are turned on. This is best achieved by using V_hi voltage values which are much lower than Vg, so all devices – including the last one in the chain – are in the linear regime.

To determine best test conditions, a series of preliminary tests were performed on Gated Contact Chains across the wafer processed with FinFET technology. The results are shown in Fig. 5, where row traces of I-V characteristics are shown for two Vg values. Two groups of traces can be distinguished, but it is not easy to set the spec limits to distinguish between devices with good and bad behavior. The separation between the devices increases as Gate Voltage increases.

Fig. 6 shows a variability plot for Chain Currents collected from a different FinFET process on various N-type structures with 400 segments. The structures were measured under various V_hi/Vg conditions. The Gate and the Well currents are also measured for every chain, and structures showing high values of these currents are filtered out from analysis with the assumption that the failures are not related to contact failures.

It should be noted that the resistance of Gated Contact Chains is much higher than that of typical passive chains, and the chains with 1-Fin devices have highest device resistance contribution among all chains. In early development, when Vt distribution is still quite wide and variable, the chain size may be limited to several hundred, or even several tens of contact links. This severely impacts observability and capability of detecting bad contacts. To account for small contact chain size, the number of chain replicates needs to be very high,

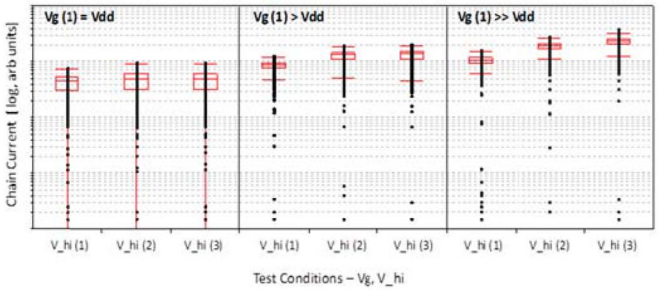

Fig. 6. Response matrix of chain current at various V-hi under different gate voltage overdrive conditions. The distribution tale is modulated by test conditions boxplots show quartiles and extensions of 1.5× interquartile range.

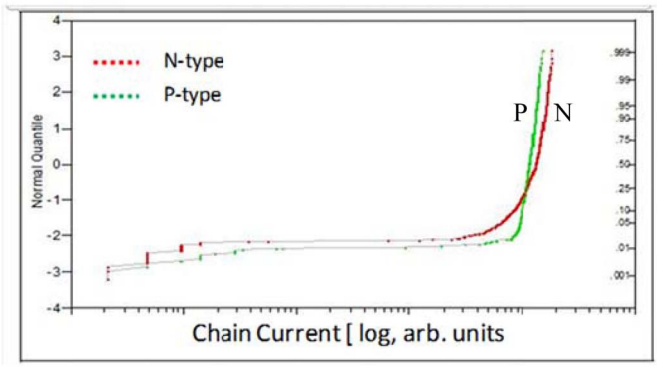

Fig. 7. Distribution plots of the current from N and P-type contact chains. Test conditions Vg(1)/V_hi(2) in Fig. 6.

and that is becoming a roadblock due to design constraints - the area overhead due to test structure pads becomes a limiting factor in reaching high structure count in a test chip. One possible solution is to use an addressable array of Gated Contact Chains, each having a small number of contact links, similar to the solution described in [10]. We will further discuss such implementation in Section V.

III. Results

The results presented here are from a FinFET process developed on "bulk" substrates with junction/well isolation (similar to that described in [6]). High-k dielectric with Metal Gate was implemented through Replacement Metal Gate process. Both N- and P-type devices had epitaxially grown raised Source/Drain regions with W contacts.

Wafers were tested after Metal1 metallization. Multiple test structures were measured per each die, and all dies were tested for increased statistics and wafer failure maps. The test was executed on an internally developed parallel tester [11].

A. Identification of Failing Structures

The Gated Contact Chain described in this paper is a suitable tool to capture true failure modes impacting contact yield in fully processed integrated circuits. Unfortunately, these structures can also fail due to other failure modes, not related to the contact. Low current in the chain can be caused not only by an open or resistive contact, but also by a poor performance of one of the transistors connected in series in the chain. As an example, gate dielectric failure can kill the device so it cannot be turned on, resulting in a high chain resistance.

Another failure mode impacting contact chain tests is junction leakage. When there are problems with junction isolation and high junction-to-well leakage (e.g., with silicide problems), the current measured at the High Pin terminal may not represent true chain resistance, and may be dominated by a junction leakage component. This will result in incorrect classification of the contact chain status, even in case of a failing contact.

In order to identify failing structures, the following procedures were used in the analysis flow:

- A data filter was applied first to identify structures failing either gate current leakage, or junction leakage criteria, since such structures would not be capable to detect contact open failure
- The remaining structures were classified into "Pass/Fail" categories using arbitrary specification limits (depending on device type and contact experiments)

An example of the results for one particular design experiment is shown in Fig. 7. The optimal test conditions were chosen based on data from Fig. 6.

Cumulative plots of Chain Current collected under the optimal test conditions are shown for Gated Contact Chains with both device types, and high resistive tails can be isolated with appropriate I_hi current spec limits. Typically, two sets of specs are used – for the Hard Failures (complete opens), and also for the so-called Soft Failures (highly resistive chain). The soft failures are usually a subject to more detail characterization with additional tests.

B. I-V Trace of Failing Structures

Once the Gated Contact Chain is identified as "Fail", it can be further investigated with additional measurements to determine failure mode.

Examples of the output Current-Voltage characteristics of the Gated Contact Chains are shown in Fig. 8. Two types of characteristics are found, confirming the "Pass" and "Fail" test structure classification.

"Pass" structures show large I_hi current with a weak V-hi voltage dependence – this is the expected behavior since the test conditions under increasing V_hi voltage push the chain current from the linear into the saturation regime (to use the MOSFET analogy) and the chain current saturates at a constant value. In contrast, the "Fail" chains have low I_hi current and show no sensitivity to V_hi voltage. Some of the structures show exponentially increasing current behavior which may indicate junction leakage. More studies are needed for that type of failure, as it may not be related to contact failure, and may impact the test results depending on the test conditions used for failure detection.

Fig. 9 shows transient Current-Voltage characteristics, where gate voltage was swept with V_hi terminal kept at constant voltage. Three distinct behaviors can be seen in this graph, represented by the curves chosen from three dies.

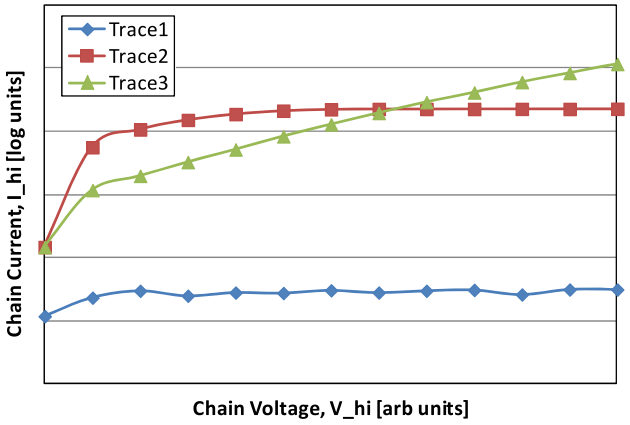

Fig. 8. Output characteristics of gated contact chain structures measured at constant gate voltage.

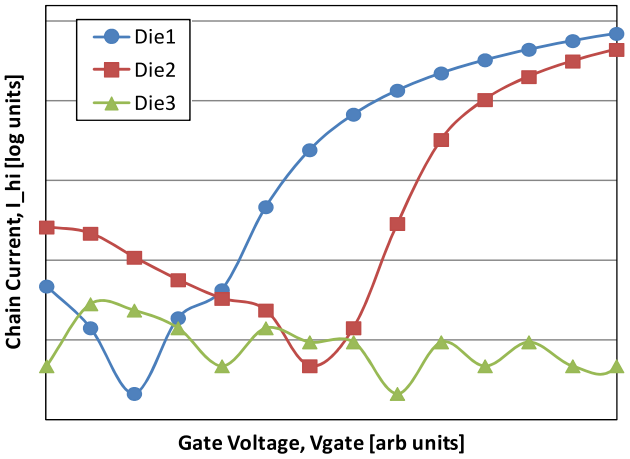

Fig. 9. Transient I-V curves measured on failing gated contact chain structures. I_hi(Vg) characteristics show three types of behavior, depending on failure mode. Die 1 represents the expected characteristic of a "Pass" chain.

They can be classified as follow:

- "Pass" structure (Die1) which has the expected chain resistance and shows Chain Current in the expected range, above the fail spec limit
- "Fail" structure (Die2) failing due to a bad transistor, causing chain resistance to be high at intermediate test conditions. Possibly, one of the transistors in the chain has high Vt and limits the Chain Current at test conditions. Increasing the Gate Voltage eventually turns the transistor ON and the resistance decreases
- "Fail" structure (Die3) failing due to a very high chain resistance caused by bad contact. The current value here is insensitive to the gate voltage.

IV. Discussion

Through the process of conceiving and designing Gated Contact Chains, we gained significant experience in designing test structures to characterize contact failures in FinFET technologies. It required trade-offs between detectability and observability.

First, the contact failure needs to be characterized in the terms of its sensitivity to design attributes, i.e., is the failure caused by random occurrence, or is it driven by one of the attributes of its design. So the test structures need to cover a wide range of attributes across the layout factors, among them:

- contact type – P vs N
- number of Fins and the size of the contact
- gate pitch – space between gates where epitaxial Source/Drain junction material is grown
- contact density
- contact space to the gate (most of contacts have a minimum space to the gate, but it is important to understand the process window)

The attribute dependence, listed above, requires large number of separate tests structures, each sensitive to a separate attribute. To provide adequate failure rate observability across each design, multiple replicates of each contact chain design need to be placed on silicon and tested for possible failure. High observability across wide range of test structures with different design attributes requires implementing very large number of contact chains on limited silicon area, available on a test chip. This can be realized using high density test structures, which minimize the impact of the test pads. In typical implementation of the contact chain test structure, a 2- terminal chain is used. With a Gated Contact Chain, 3 or 4 terminal connection is needed, and the chain size is limited to several hundred contacts. In order to achieve the observability of failure rates needed to support good yields of the product (parts per billion), one would need to use a very large number of structures with prohibitively large area (pad size limited). To mitigate this problem, we need to implement the gated contact chains as part of addressable arrays. It is also possible to design smaller chains to be used in such arrays as "micro device arrays". In such configuration each Gated Contact Chain structure can be treated as a single transistor device, and tested for a drive current. Each failing device can then be further tested to identify a failure mode.

To enable such capability, our test strategy provides multiple test scans on structures failing the initial test. The secondary test collects complete transient (I_hi vs Vgate) and output (I_hi vs V_hi) characteristics – as shown in Section III-B. It also includes testing the Well leakage (a separate Well terminal may be needed in the structure design).

As mentioned in earlier sections, the interpretation of test results of the Gated Contact Chains is not a straight-forward task. The chain failure may involve multiple failure modes, and the chain can fail for multiple reasons, not all of them caused by a contact itself. Extensive work is needed to develop a test and analysis algorithm to identify the failure mode. Fig. 10 illustrates some of possible failure modes affecting Gated Chain test behavior, and Table I summarizes electrical responses and their interpretation.

The table shows only some of the main failure modes, obviously, the structures can also fail from some other defects, not specific to the test structure design. Expanding the DoE of test structures across layout attributes helps to identify common

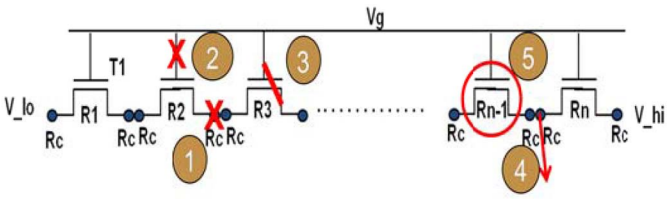

Fig. 10. Illustration of possible failure modes impacting electrical response of the Gated Contact Chains. The numbered circles indicate failure modes explained in Table I below.

TABLE I
SUMMARY OF FAILURE MODES AFFECTING ELECTRICAL CHARACTERISTICS OF THE GATED CONTACT CHAIN STRUCTURE

#	Failure Mode	Structure Response	Interpretation	Comment
1	Open Fin Contact	Very high resistance	Open Fin Contact	Intended fail detection
2	Open Gate Contact	Very high resistance	Open Fin Contact	Difficult to detect Not a common failure mode
3	Contact to Gate short	High Gate Current Chain current may reverse direction and increase value	Gate short to S/D or channel	The response depends on Vg and Vdd conditions
4	Gross Junction leakage	Increased Chain current	Junction leak Vt shift across all devices	Not a concern in FinFET on SOI
5	Gross Vt shift	Large shift in Chain current	Single device failure High Vt across all devices	Need additional diagnostics

systematic failure modes as well as random component due to defects, particles, etc.

V. FURTHER TEST STRUCTURE IMPROVEMENT

One of the limitations of the approach described in previous sections is poor observability, as the number of contacts in each chain is very limited. Since each DUT requires separate sets of pads, the area efficiency is rather poor. One of the solutions can be a usage of an addressable array, like the one described in [10] and [12] for statistical transistor characterization, and shown in Fig. 11.

In such array, number of pads is greatly reduced, and the total number of contacts tested for failure can be significantly increased by replacing discrete transistor DUT's with Gated Contact Chain structures. By using such addressable arrays, we increased 8X the number of contacts per test structure area (assuming the same test structure footprint on the wafer).

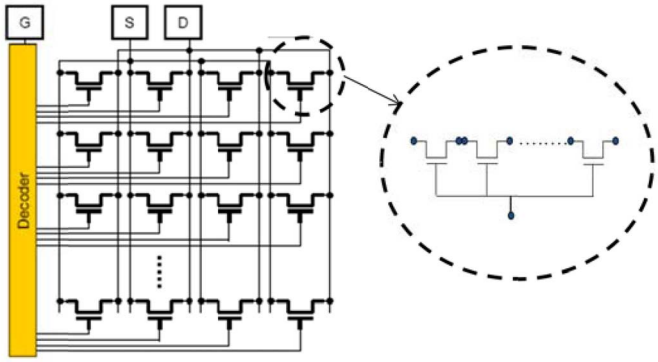

Fig. 11. Addressable array for transistor characterization. High contact failrate observability is supported by replacing discrete device with a gated contact chain structure.

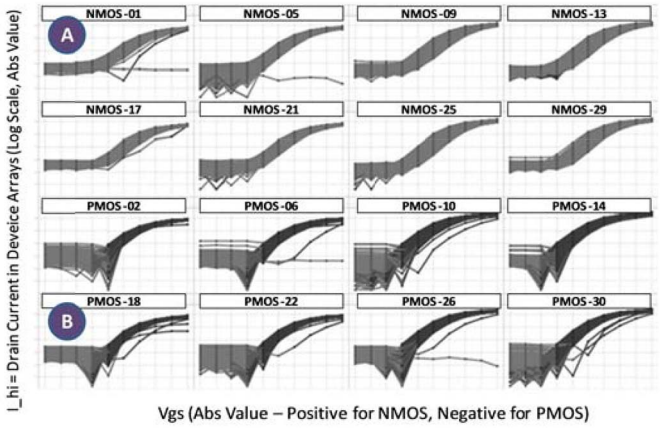

Fig. 12. Examples of I-V curves collected from gated contact chains implemented in active arrays. Each tile represent 512 DUTs with different design attributes, for NMOS and PMOS (as marked on the labels).

Extensive tests and characterization, combined with the large number of unique test structures (to address design attribute sensitivity), puts strong requirements on the test speed and throughput. In our designs, we take advantage of highly parallel testing capable of both low-current single-point-test, as well as high speed I-V sweep measurements across multiple test channels.

I-V characteristics presented in Fig. 12 capture some abnormal behaviors, similar to those seen earlier on discrete chains in Fig. 9. Each tile in the graph contains a sample of curves collected from 512 Devices-under-Test (DUTs). In addition to the failing chain, (identified based on resistance distribution for all DUTs), we plotted multiple characteristics from other healthy structures – this helps to identify an outlier curve with abnormal contact resistance or transistor Vt shift. Further analysis of the outlier behavior helps to classify the failure mode, along the fails identified in Table I. We highlighted two tiles in Fig. 12 – one for n-type array (marked A) and one for p-type (marked B).

Fig. 13 presents I-V traces of those DUT's in linear scale, so it is easy to see polarity of the current measured at the Drain terminal (I_hi of the Gated Contact Chain).

- the graph marked A shows two failing devices, one due to an open contact fail, and the other due to Gate-to-Contact

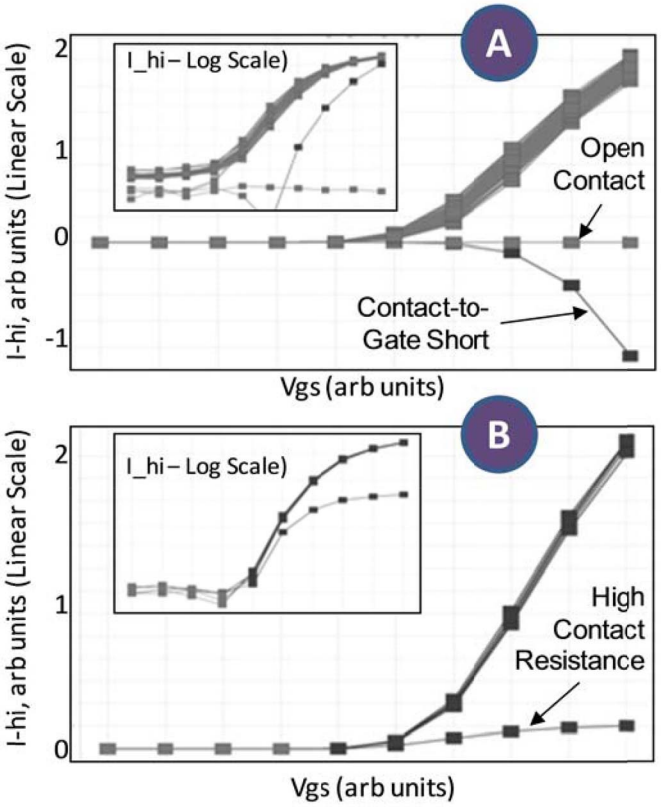

Fig. 13. Detail traces of the failing structures from the panels A and B in Fig. 12, shown together with traces of good DUT's, measured in the same array. The main graphs show the plots in linear scale, to show the current polarity, while the inserts show the same plots in the log scale.

short (because Gate potential rises higher than "Hi" terminal potential, the measured current polarity is opposite to that of good, healthy structure)

- B-marked graph illustrates typical example of the high resistive Contact, clearly visible on linear scale plot (log scale plot confirms that the devices in the chain turns-on properly at the same voltage as in good DUTs.

The results above confirm functionality of the active addressable arrays and applicability of the proposed solution to increase density and observability of test structures with Gated Contact Chains.

Another characterization aspect worth addressing is localization of a defective element for failure analysis. In case of the "passive" contact chain, when the chain may contain tens or even hundred thousands of contact plugs and cover an area of hundreds square microns, the only way to find an open contact is to use e-beam tool (electron microscope) in Voltage Contrast mode. In fully processed wafer it requires de-processing down to lowest metal level (upper runner level, as shown in Fig. 1) and skillful use of Active or Passive Voltage Contrast to find a failing link, in which one or both contacts can contain defects. Alternatively, the wafer can be de-processed to Contact level, exposing the Contact plugs. The contact array of the failing chain (identified from electrical test) can then be scanned in Passive Voltage Contrast mode to find a bad contact.

Gated Contact Chains would use similar approach to localize a failing contact. Voltage Contrast can be used to localize the defective contact, however, the scan time may be much faster than in case of "passive" chain. This is because the area of the Gated Chain DUT is much smaller - usually is limited to less than 500 contacts within a small area of few square microns. As discussed earlier, an addressable array is used to test large number of such small DUTs, and the failing DUT can easily be localized within the array.

VI. Conclusion

Characterization of failure modes (specifically contact failures) in advanced silicon technologies is becoming an increasingly complex task. The proposed Gated Contact Chain allows true assessment of the contact failure modes, and provide reasonable failure rate observability, although special techniques are needed to resolve trade-off problems. In our work we proposed test structures that are suitable to detect all major contact failure modes, and isolate them from other failure modes, impacting contact fail detection. We also demonstrated feasibility of using such structures as DUT's in active addressable device arrays, earlier developed for statistical device characterization. Finally, the developed method can easily be implemented as a practical solution into the mass production diagnostics toolset, which can provide high observability of the contact failure rates.

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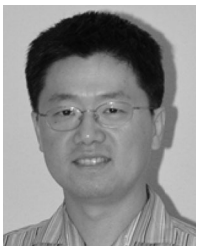
Stephen Lam, photograph and biography not available at the time of publication.

Shia Yu, photograph and biography not available at the time of publication.



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