Design and Measurement Requirements for Short Flow Test Arrays to Characterize Emerging Memories

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***Abstract*— Emerging non-volatile memories are becoming increasingly attractive for embedded and storage-class applications. Among the development challenges of Back-End integrated memory cells are long learning cycle and high wafer cost. We propose a short-flow based characterization of Memory Arrays using a Cross Point Array approach. A detail analysis of design requirements and testability confirms feasibility of the short-flow based solution to reduce Turn-Around Time and development costs.**

***Index Terms*— Emerging Memories, Cross Point, Memory Arrays, Cell Characterization, MRAM, PCRAM**

I. Introduction

THE embedded non-volatile (NVM) memory market traditionally has been dominated by embedded Flash, based either on Floating Gate or Charge Trap SONOS technology. There have been multiple reasons for new contenders for NVM applications. The new candidates use other mechanisms to store information, are faster than traditional charge-based memories, and operate at lower voltages, lower power, and higher speed. Another reason which favors new memories is process simplification and mask count reduction. From integration and scaling perspective there are significant challenges to integrate embedded Flash into a technology with a High-K/Metal Gate, required for advanced logic nodes [1-2]. Processing them together on the same wafers may have potentially negative impact on yield, reliability, and cost. New emerging memories embedded in the Back-End-of-the-Line (BEOL), between metal layers, allow decoupling memory cell module integration and limit the impact on original logic technology platform and transistors.

Such BEOL-embedded non-volatile memories have already been proven as stand-alone memories (e.g., MRAM, ReRAM, or PCRAM) and some are already in development or early production for embedded applications. BEOL integration helps to keep FEOL/MOL of original logic platform unchanged and also reduces integration cost (only 2-4 extra masks compared with >10 for embedded Flash), operating voltage, power consumption, and speed [3-4].

From a development perspective – integration, optimization, and reliability demonstration with Cu-based BEOL process remain the main challenge. At the same time, complex layer processing and material optimization consume extensive learning cycles, as most of the manufacturing fabs are not set up for development and characterization work.

II. New Memory Cell Development

A. Memory embedded into Logic platform

Embedded memory products are usually build by adding a memory blocks and all supporting components onto already existing and qualified logic technology platform. In case of traditional flash memory embedded into Front-End-of-Line (FEOL), the changes to existing integration and impact on devices are very significant, and the whole technology requires re-integration, re-characterization, and re-integration.

Development and manufacturing ramp of a product with new, BEOL-integrated emerging memory is probably an easier and less complex task, since it does not require re-developing FEOL modules. Still, it needs an extensive characterization and improvement work on BEOL and memory cell itself, involving material optimization, module integration, process adjustments, and co-integration with logic blocks.

In typical development, the initial integration work focuses on patterning and layer stacking constructional tasks which can be performed at module level, with short flow validation using planar imaging, cross-sectional analysis and metrology. More advanced characterization requires wafers for electrical measurements. Some of the wafers, used for single Bit Cell characterization, can be processed as a short flow, with test

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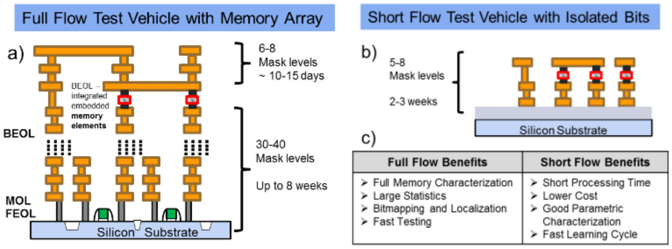
structures providing direct connectivity to selected Bits in array structure [5]. Those tests allow early memory characterization; they also enable coarse optimization of the materials, unitary process steps, thermal cycles, etc. Such approach, however, provides very limited statistics of the bit performance or bitcell yield and reliability (see Fig. 1).

To gain more insight into the memory yield and systematics, fully testable memory arrays are needed. Emerging memories, although integrated between BEOL Metal layers, need logic devices as selectors, and to support memory periphery and I/O operations. To build fully addressable arrays, the wafers need to be processed through the whole FEOL/MOL process. After that the lower Metal levels with embedded memory module are processed, and finally the upper Metal levels are created to connect memory blocks and logic periphery, route the power, and provide connectivity to I/O pads. This is a typical practice in technology development, where fully processed wafers are used to test memory cells and addressable memory arrays.



Full Flow Benefits	Short Flow Benefits
➢ Full Memory Characterization ➢ Large Statistics ➢ Bitmapping and Localization ➢ Fast Testing	➢ Short Processing Time ➢ Lower Cost ➢ Good Parametric Characterization ➢ Fast Learning Cycle

Fig.1. Comparison of processing complexity between (a) – Full Flow test chip for BEOL-embedded memory and (b) Short Flow test chip. The table shows difference between benefits for each of them.

They provide not only bitcell parametric information, but also failure bit statistic, which is needed to determine bit yield and to build failure mode pareto. Such information is needed to understand systematics and process window across array, reticle field, and wafer regions. Logic and Memory testers are used to collect the yield and performance data of memory cells, and to assess reliability.

In some embedded applications, memory elements are placed at high interconnect levels, even above Metal 5 [6, 7]. Processing the wafers through FEOL, MOL, and multiple metal levels significantly increases processing time and wafer cost during technology development and ramp of embedded memories. For that reason, development teams often use a short flow processing to build only a subset of the integrated flow, containing the layers with memory elements. The short flow can be used to optimize some of the processing steps, even after main integration project has been completed. Such approach, however, rarely can provide any electrical data.

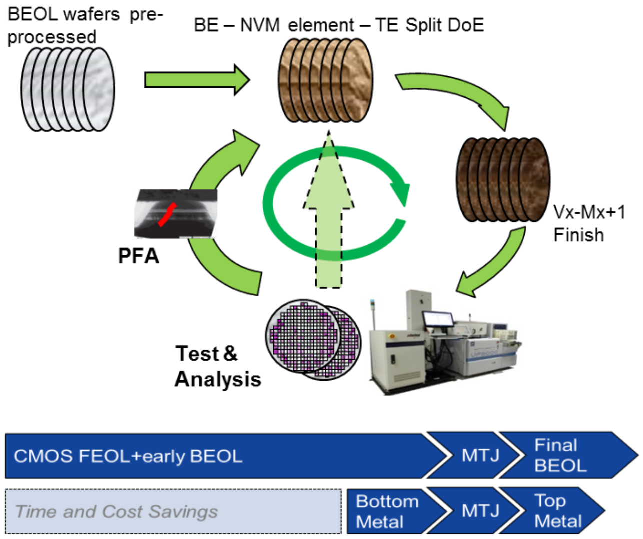


Fig. 2. Short Flow test vehicle for memory element test enables faster learning cycle and lowers the development cost compared to full flow wafers with integrated memory process. Bottom graph shows potential time saving and impact on learning cycle of embedded MRAM module using Short Flow approach.

B. *Memory characterization with short flow test structures*

As mentioned earlier, complete characterization of the memory cells requires full memory array of desired size and logic-based periphery for Row/Column selection, read circuitry, etc. The memory testing involves writing various patterns to understand cell interaction, detect failure modes and possible spatial signals, caused by cell placements, or Row or Column interaction, and possible disturbs during Program, Erase, or Read operation. Fully processed arrays are needed also for reliability tests - endurance and data retention.

A test chip which can be run and tested in a short flow mode is an attractive alternative. Although not fully functional, it can provide information about the memory element performance, yield, and fundamental reliability properties while also being cheaper and faster learning tool. The shortening of the learning cycle and saving benefits are shown in Fig. 2. Short flow solutions have been already proposed earlier to screen materials and collect basic electrical parameters [5]. While they can support initial development, data volume is limited by the test element count and the throughput of the parametric tester, and the resulting test data statistics are usually insufficient to drive technology development, memory cell optimization, and process improvement. To make a short flow test vehicle more effective, a rich statistical data collection approach using high density test structures (arrays) is needed. We proposed such an approach to characterize memory elements using short flow test vehicle using cross-point arrays, as shown in Fig. 3 [8]. The arrays can be used to collect the data on large amount of bits, check execution of program/erase functions, and measure cell resistance in each of states. For efficient testing, this approach requires a flexible, fast, and highly parallel parametric test system for simultaneous probing of multiple structures [9].

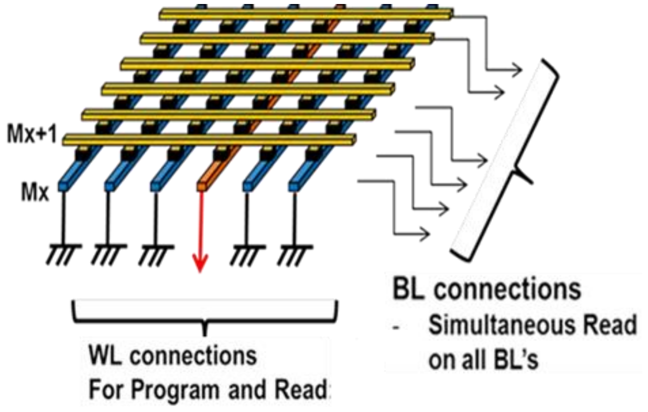


Fig. 3. Cross Point array of memory elements with simultaneous measurement of multiple elements using parallel test. The memory elements are at the cross-point locations between lower level WL's and upper level BL's

There are two consequences of using the short flow and skipping the most of the process flow.

The first one is a connectivity of the array. In order to make it electrically testable, a special array need to be built, using dedicated wiring, and with different test pad access for wafer probing. The arrays, however, need to represent real product array layout, with the same cell integration between upper and lower metals, the same cell size, distances, pitches, and placement across the array. Without that, the value of the test data would be rather limited and not representative.

The second consequence is a limited test coverage. The testing of cross-point arrays cannot be done with a memory tester (since there are no Row/Column decoders), so parametric tester with a pulse generator needs to be used. However, it should be noted, that the short flow test arrays do not need to be tested in exactly same way as the product arrays to provide feedback useful to process and device engineers. We can define the objective of test arrays in terms of partial memory characterization, and set success criteria based on detection of bad bits. For that, the test needs to be able to find and localize bitcells which are either open, shorted, or those which cannot be switched between two logic states, represented by high-resistance state (HRS) and low-resistance state (LRS).

C. *Test challenges of passive cross-point arrays*

Cross-point architecture has been discussed as a candidate for high density memory arrays and the problem of "sneak path leakage" impacting read margins is widely discussed in the literature [10, 11, and references therein]. Fig. 4 summarizes this problematic issue.

The array seen in Fig. 4 is a schematic representation of the construct from Fig.3. Let us consider a resistance test of the specific cell located at the intersection of WordLine WL3 and BitLine BL4, marked by the circle.

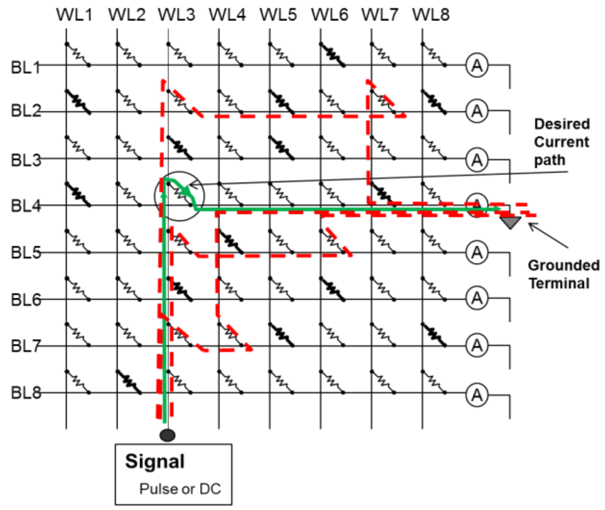


Fig. 4. Sneak leaky paths in cross-point array and their impact on resistance measurement of the selected cell. The schematic symbols of the resistors at the crossing of BL's and WL's illustrate cell resistances.

In two-terminal configuration, with read voltage ("Signal") applied to WL3, and the current measured on grounded terminal of BL4, the resistance calculated is not just that of a single cell. This is due to additional current paths, their examples illustrated by dashed lines; there are many of such "secondary" paths and their number increases as the array size increases. These secondary paths are called sneaky leak paths. Each of them is a path through 3 cells, so the current through a sneaky path is usually much lower than through the selected cell, but the overall effect may be very substantial, due to the large number of such paths. Hence the resistance measured between single selected WL and single selected BL can be significantly lower than the resistance of the selected cell. An additional selector element has been proposed to block the sneak paths and allow larger array size [10, 11]. Most embedded memories, however, use a silicon device selector (diode or transistor), which is not readily available in BEOL short flow. Therefore, the proposed arrays need to use a different approach to mitigate the risk of sneak leakage paths.

Let us consider the ideal cross-point array, with zero-resistance WL's and BL's (no parasitic resistances), which is tested according to the conditions depicted in Fig.5. With a single WL at the Read Voltage ("Signal"), and all other WL's at ground potential, and with all BL's also at ground potential, the only existing current paths are direct paths through the selected cells of WL #3, and currents uniquely represented by values measured at the BL's terminals. All "secondary" current paths are shut down, because the potential differences across all other cells are zero.

In conclusion, with the array as in Fig. 5 and with proper test setup (multi-channel parallel tester and pulse generator), it should be possible to measure initial resistance of all the cells, and check if they are fully functional.

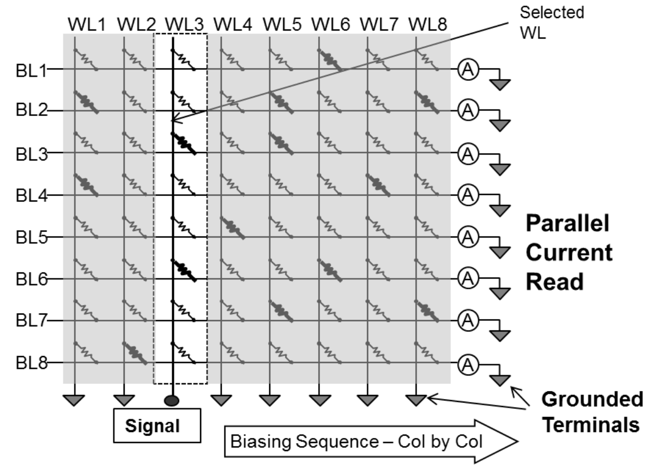


Fig. 5. Simplified schematics of a cross-point array. During the measurements, all BL and WL terminals, except for Selected WL, are connected to ground potential.

To achieve this goal, all cells of the array can be programmed into one state, tested for resistances of all elements, then programmed into another state and tested for their resistances again. Since the resistance of each cell can be tested independently, the array can provide valid, bit level information about cell functionality. The statistical size of the data population will depend on the size of the array, and the number of the arrays tested, either in series or in parallel. Therefore, the benefits from building larger cross-point arrays is obvious for multiple reasons: (i) more cells can be placed in a single test structure using the same number of probing pads; (ii) test time per cell can be shortened by testing larger number of cells on the same WL; (iii) larger number of test arrays that can be placed per die, resulting in higher overall fail rate observability per die and per wafer.

There are, however, significant drawbacks of increasing the array size. As mentioned earlier, the case discussed in Fig. 5 was an ideal case. In reality, the cross-point array of cells sandwiched between two conductor layers has many parasitic resistances, some of them localized, and other distributed. Because of them, the assumption about zero potential difference across all unselected cells is not valid [12].

With increasing distributed resistance between the cells along WordLine and along BitLine, the problem becomes significant - it starts impacting measurement accuracy and capability of detecting the resistive state of the cell (especially for low resistive memories, like MRAM). Moreover, increased array size, having more WL and BL connections, requires more probing pads, thus increasing distances and resistances between the array and pad contacts to the tester. Voltage drop along these external array connections causes additional uncertainties and errors in test condition assumptions.

Fig. 6 shows schematics of the equivalent circuit of the array, which takes into account parasitic resistances of the design of the test structure. Clearly, the I_{BL} current measured at each of BL terminals is not just a function of the V_{on} voltage and Cell resistance, but many other parameters.

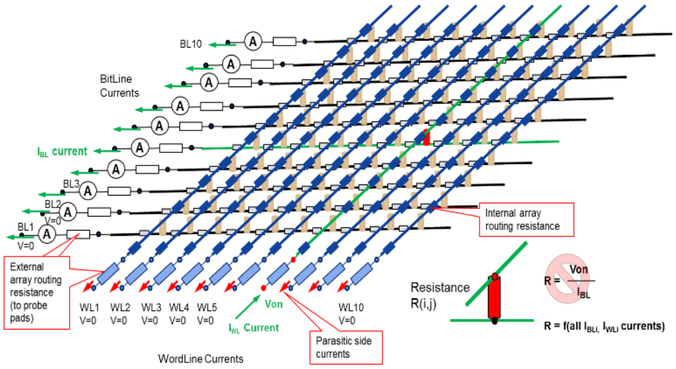


Fig. 6. Schematics of a cross-point array with internal and external parasitic resistances. BL/WL current meters represent parametric test (with multi-channel tester). The lower-right corner insert shows the resistance of the selected Cell – this resistance cannot be simply calculated from V_{on} applied to the WL and resulting BL current I_{BL}

III. Cross Point Array Test Simulation

A. Array modeling for cell resistance extraction

As discussed in previous paragraph, parasitic resistances, both internal and external to the array, contribute to the errors in determining the resistance of array elements. The parasitic resistances are showed in Fig.6, along with the test conditions and currents measured on Array terminals. Typically, only the BL currents are measured to calculate cell resistances. However, in order to estimate the errors, we propose to measure the currents on all WL's as well.

The problem becomes easier to solve when the values of parasitic resistances, or at least their estimates are known. Using the values of the currents measured on all array terminals, and parasitic resistances (from the design), we can solve circuit equations and get all node potentials and all internal currents flowing between the nodes.

In current work, we focused on test simulation and analysis of cross-point arrays without selectors, as well as their optimal design. To support this study, we built a circuit simulator and a solver which first generates parametrized distributions of cell resistance in the array, and then simulates the test results taking into account parasitic resistances and their variability.

The internal and external resistances are both design dependent, and can be varied within wide range, but they are difficult to minimize. Precise knowledge of their values helps to extract the cell resistances with good precision. Hence, using a circuit modeling in combination with all-terminal current measurement data, we can minimize errors caused by sneaky paths and background currents. The solver calculations can be added to test program, and post-processing algorithm can be used for cell resistance extraction after the test.

Considering the objective of using passive cross-point array to test emerging memory cells, we should ensure that the proposed approach can test and extract the following:

- Initial resistance of the memory cells
- Cell resistance after Program and Erase operation (or SET and RESET)
- Identify and localize the cells which cannot be programmed or erased (Stuck at LRS or HRS), or the cells with low HRS/LRS resistance ratio

B. *Impact of design parameters and parasitic resistance*

As discussed in Section II, minimized parasitic resistances are beneficial to reduce sneaky leakage paths. Further improvement in precision of determining cell resistances should come from test and circuit simulation. There are several assumptions about the array design and test [13]

a) in order to reduce voltage drop along the current paths, we assumed that the array is designed with low resistance between neighbor bits, both along WL as well as BL (called later “Link R”)

b) we also assumed that the access pads and wiring leads from the pads to the array BL and WL terminals is minimized and equalized (called later “External R”)

c) parallel parametric tester is used to simultaneously measure the currents on all BL’s and WL’s (this is the largest differentiator and method enabler - in real memory circuit sense amplifiers are used to detect High/Low resistance state of the cell)

In addition to parasitic resistance we also need to account for resistance variability and voltage variability caused by tester channel mismatch.

To estimate the impact of all sources of errors, we performed several simulations. We used circuit simulator to simulate the currents and circuit solver to back-calculate node potentials and array resistances. The simulation flow is illustrated in Fig. 7. Its steps can be summarized as follow:

1) generate desired distribution of cell resistances in the array (in most cases 10 x 10 array)

2) generate random distribution of parasitic resistances around nominal design targets, and voltage offset for ground potential

3) perform circuit simulation for multiple bias conditions, sequentially applying bias to every WL, and for each run calculate a set of current values for BL’s and WL’s

Each set of calculated current values represents the data hypothetically measured by tester. This set of current values is then used as the input to circuit solver program to extract all cell resistances in the array. The extractions assume nominal values for all parasitic elements and no voltage offset.

The cell resistances obtained by such “back-calculation” approach were then compared with initial input values and errors were calculated.

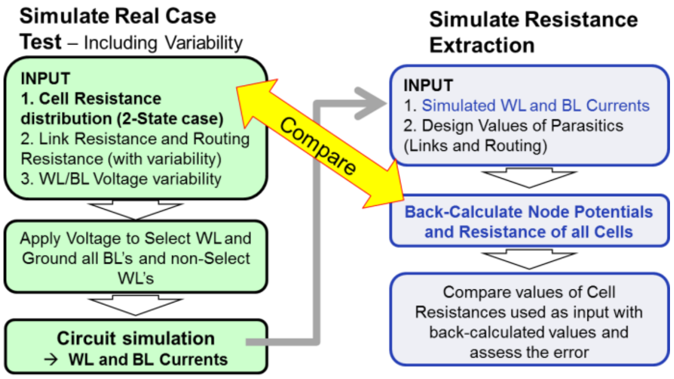

Simulate Real Case
Test – Including Variability
INPUT
1. Cell Resistance distribution (2-State case)
2. Link Resistance and Routing Resistance (with variability)
3. WL/BL Voltage variability
Apply Voltage to Select WL and Ground all BL’s and non-Select WL’s
Circuit simulation
→ WL and BL Currents
Compare
Simulate Resistance Extraction
INPUT
1. Simulated WL and BL Currents
2. Design Values of Parasitics (Links and Routing)
Back-Calculate Node Potentials and Resistance of all Cells
Compare values of Cell Resistances used as input with back-calculated values and assess the error

Fig. 7. Simulation flow to estimate cell resistance extraction errors

We performed circuit simulation for two types of emerging memories with distinctive resistance ranges. For MRAM memory cells we assumed 1 kΩ for LRS and 2.5 kΩ for HRS, and PCRAM with 30 kΩ for LRS and 2 MΩ for HRS, respectively. For each case, the resistance distributions were randomly generated for high and low resistance state, and Cross Point arrays of 10x10 elements were built. The arrays design is assumed to minimize internal WL/BL resistances (called here “link” resistances). To check their impact we assumed two cases: 2 Ω and 20 Ω.

The results are shown in Fig. 8 and Fig. 9. For the nominal case, with no variability, the extracted cell resistance values (from back-calculation) were found to be close to their original input values, even for 20 Ω array Bit-to-Bit link connections (see the case of PCRAM in Fig. 8). For MRAM, low resistance memory, the effect of link resistance is much stronger, with errors as high as 5-10% for 20 Ω links (Fig. 9).

The predictions are quite good when the Link resistance has no variability. Additional variability introduces an extra error. For high resistance PCRAM, the error is relatively low - below 1% (Fig. 8) even with highly variable (30%) link resistance. The same link resistance variability can introduce 5-10% error in estimating cell resistance in low resistive memories, like MRAM (Fig. 9). The test results are also very sensitive to stability and magnitude of the offset voltage of the BL ground source, which can drive the error to 20% and above, especially for high resistance memories (see Fig. 8 for PCRAM). The reason for such high sensitivity to the offset is the background leakage currents flowing from neighbor BL

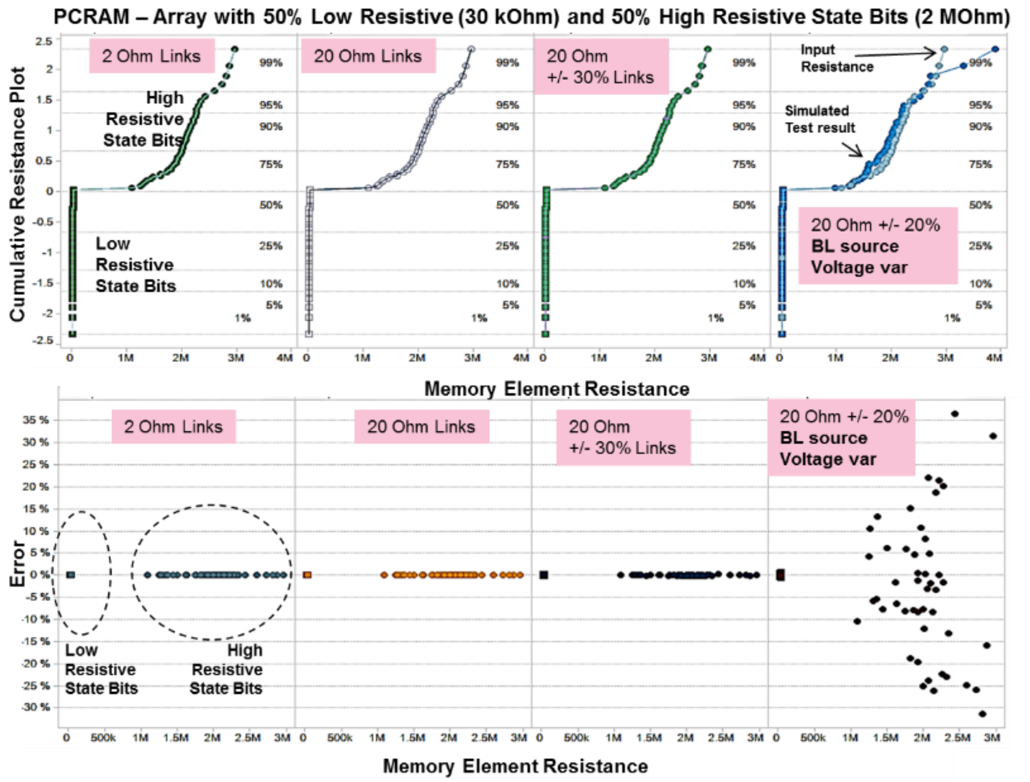


Fig. 8. Test result simulation for PCRAM Cross Point array with Set (30 kΩ) and Reset (2 MΩ) Bits. Upper plots show Input resistance values and their back-calculated counterparts, and the lower panel show the errors in estimation of resistances. Four panels represent various array design and test conditions

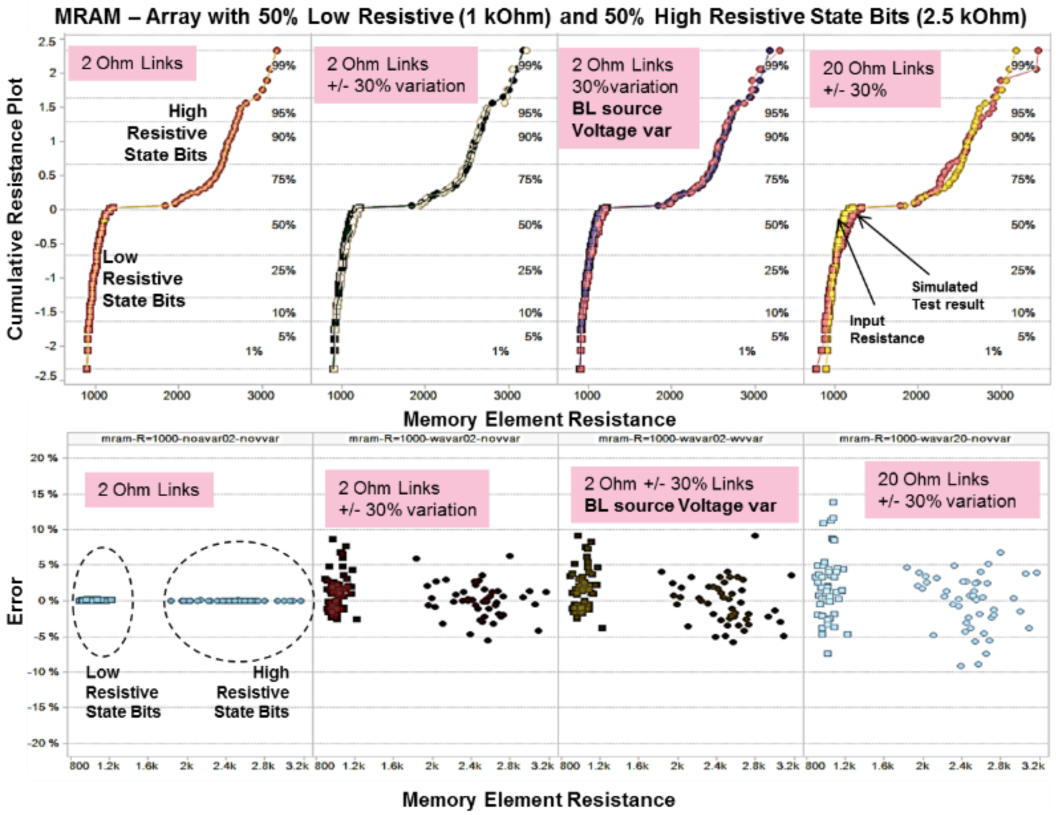


Fig. 9. Test result simulation for MRAM Cross Point array with Low Resistive (1 kΩ) and High Resistive (2.5 kΩ) Bits. For such low resistance memory cell test the Link resistance introduces additional error of 20-30% (especially when the resistance has high unaccounted for variability). The effect of BL ground potential offset is negligible.

terminals (in the presence of low resistive cells) into the select BL terminal associated with the high resistance cell.

C. Bad bitcell detection

One of the examples of usage and application of array test structure is detection of bad bit which cannot be toggled between Low-Resistive and High-Resistive states. This capability is absolutely necessary, since quite often bad bits cannot be identified just based on initial cell resistance – as an example we can consider high resistive ReRAM or PCM cell, which cannot be classified as bad, until it fails Forming operation and programming to a Low-Resistive state.
Consequently, one of requirements for cross-point arrays is capability to distinguish between the LRS and HRS.

As found in previous simulations experiment shown in Figs. 8 and 9, uncertainty and variability of parasitic resistance significantly impact accuracy of cell resistance measurement. To demonstrate robustness of cross-point array test, even with parasitics, we performed simulations of arrays programmed to low-resistance level, as well as the one programmed to high-resistive level. In both cases we simulated the test with one bit stuck at opposite state, at 3σ value from the nominal Median of the distribution. We chose MRAM as an example for this simulation, since its low resistance cell, may be more sensitive to parasitic resistances and sneaky paths in the array.

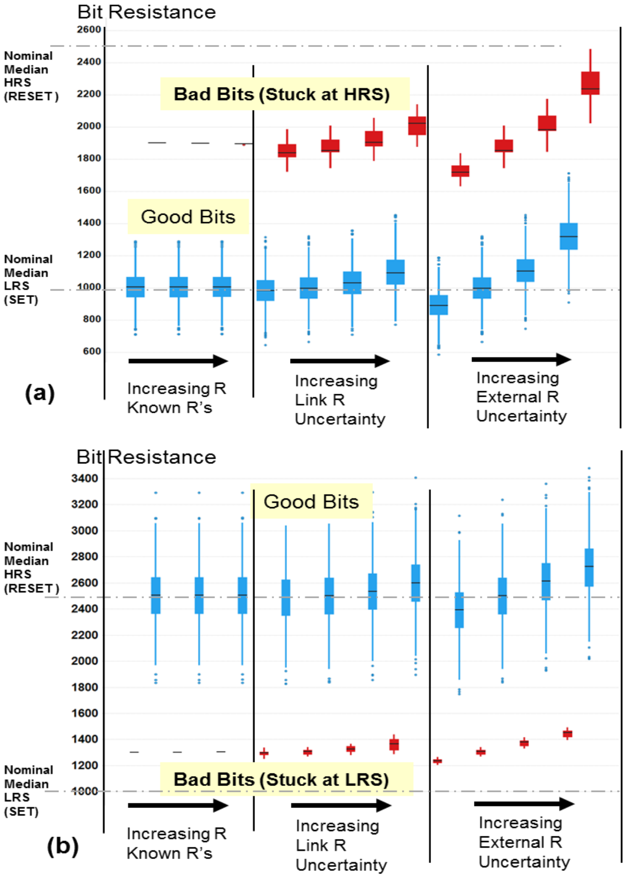


Fig. 10. Impact of uncertainty in Link Resistance and External Access Resistance values on extracted cell resistance for: (a) Error Bit Stuck at High-Resistive State and (b) Error Bit Stuck at Low-Resistive State.
The distributions of the resistance of single bad bit in the array of 100 bitcells are based on 10 simulation points

Fig. 10 shows two plots corresponding to the two "stuck at" situations. Each of the graphs has three panels presenting the results of simulation according to flow in Fig. 7:

- The first panel shows simulated test data for main LRS (for Fig. 10a) or HRS (Fig. 10b) distribution with one outlier stuck at opposite state, in the tail 3σ away from the median value, and close to the main distribution of good bits; the simulation assumes that all design parameters for Link R and External R are known and have no variability. As expected, the bad bit resistance can be extracted very precisely, with no error
- The second and third panels show the corresponding distributions with increasing uncertainty of Link R or/and External access R, when the "real" values in the array differ 20-50% from the design assumed values, with additional effect of random variability +/- 15% (as often present in real process). As expected, the additional resistance, unaccounted for, causes shifts and broadens the distributions.

From the results in Fig.10 we can see that the resistance of "Stuck at" bad bits can accurately be identified and distinguished from the main distribution programmed into the opposite state. This is especially true for bad "Stuck at LHR" bits, where the impact of parasitics and their uncertainty is much smaller than in case of "Stuck at HRS" bits. It should be noted, however, that the capability of distinguishing between the bits in LRS and HRS is not an absolute necessity for test arrays, as long as they can monitor switching between LRS and HRS for every bit separately.

D. Impact of array size

Earlier discussion pointed to the impact of the array size on accuracy of cell resistance measurement. To estimate the impact, we performed additional simulations of MRAM cross-point arrays with MRAM cells, with nominal LRS resistance of 1000 Ω, and HRS of 2500 Ω. As in previous simulation, we considered bad bits with resistance at 3s below nominal HRS, at 1900 Ω.

Fig. 11 shows the results of simulated distributions for 10 arrays of various sizes (hence the bad bit distribution includes only 10 points).

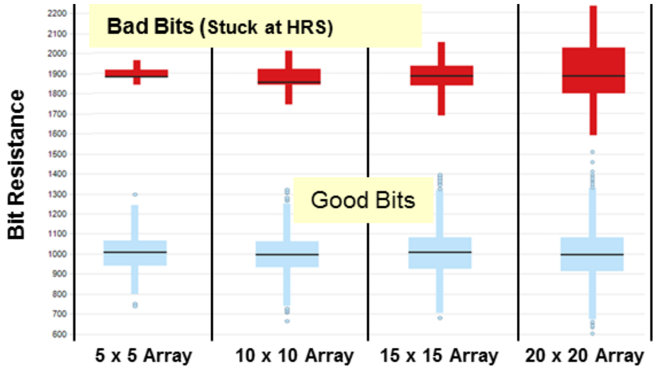


Fig. 11. Impact of array size on accuracy of bad bit resistance extraction based on multi-terminal current test and back-calculation using nominal parasitic resistance values. Array has unaccounted resistance variability for R Link and for External access resistance at +/- 15%.

In the modelled arrays the resistance of the bad bit is always the same, but the value extracted from test and corrected for the nominal value parasitics varies from case to case. "Stuck at HRS" outlier resistance uncertainty increases with the array size, and in case of the 20x20 array some of the bad bits could be misclassified, as their resistance would overlap with the perceived distribution of resistance of good bits in LRS.

The above results clearly show that the array size needs to be co-optimized with the WL and BL design, depending on bitcell resistance in LRS and HRS.

The results also prove that the test performed on cross-point arrays, even without selectors, and in presence of sneaky paths, can still distinguish between the cells with high and low resistance state, for both PCRAM and MRAM case.

To summarize, the simulations show that the cross-point array test with post-test correction (using all-terminal current measurements and parasitic resistance models) can be a robust method of identifying bit outliers and bad bits which cannot be flipped from one state into another.

Additional design efforts (BL and WL strapping) and test techniques (BL and WL resistance test, BL force potential offset compensation) can further be used to reduce the test error and provide robust test data for Memory optimization. Array size can further be optimized to provide the best trade-off between the statistical sample size of tested bits and the test speed and resistance measurement error.

IV. Conclusion

Using careful simulations we demonstrated that cross-point arrays, processed with no selectors can be used for test and statistical analysis of functionality of emerging memory cells. Multi-channel test approach coupled with proper design of the cross-point arrays can offer a good learning tool for a short flow loop characterization. This, in turn, can be used for fast and inexpensive approach for process optimization and yield improvement of new emerging memories, like MRAM, ReRAM, or PCM.

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After graduating, he was an Assistant Professor at Warsaw University of Technology, Poland. He taught academic courses and conducted research first in Warsaw, and then at University of California, Los Angeles, in the area of MOS device physics, gate dielectric characterization, radiation effects, and plasma-induced damage. After that he worked at Motorola R&D organizations in Texas and Arizona, focusing on technology characterization, with emphasis of process-induced damage and reliability.

He joined PDF Solutions in 2000, where he is now Senior Fellow. He focuses on advanced node technology characterization, methods development, and early yield ramp. Since joining the company, he led multiple projects covering Logic, Memory (DRAM, Flash), and Image Sensor.

Dr. Brozek published more than 50 papers and conference presentations, and holds several patents. He worked on numerous Committees of IEEE Conferences, among them PPID, IRPS, and EDTM.

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