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Design and Measurement Requirements for Short Flow Test Arrays to Characterize Emerging Memories

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ABSTRACT Emerging non-volatile memories are becoming increasingly attractive for embedded and storage-class applications. Among the development challenges of Back-End integrated memory cells are long learning cycles and high wafer cost. We propose a short-flow based approach for characterization of Memory Arrays using a Cross-Point Array structure and highly parallel Parametric Test. A detailed analysis of design requirements and testability, including inverse circuit simulation, confirms feasibility of the approach to reduce Turn-Around Time and development costs.

INDEX TERMS Emerging memories, cross-point, memory arrays, cell characterization, parametric test, E-test, circuit simulation, MRAM, PCRAM.

I. INTRODUCTION

The embedded non-volatile memory (NVM) market has traditionally been dominated by embedded Flash, based either on Floating Gate or Charge Trap SONOS technology. There are multiple reasons for new contenders for NVM applications. The new candidates use other mechanisms to store information, are faster than traditional charge-based memories, and operate at lower voltages, lower power, and higher speed. Other drivers for these new memories are process simplification and mask count reduction. In addition, from an integration and scaling perspective, there are significant challenges to integrate embedded Flash into a technology with a High-K/Metal Gate, required for advanced logic nodes [1]–[2]. Integrating these two technologies together on the same wafer may have potentially negative impact on yield, reliability and cost. New emerging memories embedded in the Back-End-of-Line (BEOL), between metal layers, however, enable decoupled memory cell module integration and limit the impact on original logic technology platform and transistors.

Such BEOL-embedded non-volatile memories have already been proven as stand-alone memories (e.g., MRAM, ReRAM, or PCRAM) and some are already in development or early production for embedded applications [3]–[4]. BEOL integration helps to keep FEOL/MOL of original logic platform unchanged and also reduces integration cost (only 2-4 extra masks compared with >10 for embedded Flash), operating voltage, power consumption, and speed.

From a development perspective, integration, optimization, and reliability demonstration with Cu-based BEOL process remain the main challenge. At the same time, complex layer processing and material optimization consume extensive learning cycles, as most manufacturing fabs are not set up for development and characterization work.

II. TECHNOLOGY DEVELOPMENT WITH A NEW BIT CELL

A. MEMORY EMBEDDED INTO LOGIC PLATFORM

Embedded memory products are usually built by adding memory blocks and all supporting components to an existing and qualified logic technology platform. In case of traditional flash memory embedded into Front-End-of-Line (FEOL), the changes to existing integration and impact on devices are significant and the whole technology requires re-integration, re-characterization, and re-qualification.

Development and manufacturing ramp of a product with a new, BEOL-integrated emerging memory is clearly an easier and less complex task, since it does not require re-developing FEOL modules. Still, it needs extensive characterization and improvement work on the BEOL interconnect structures and the memory bit cell itself, involving material

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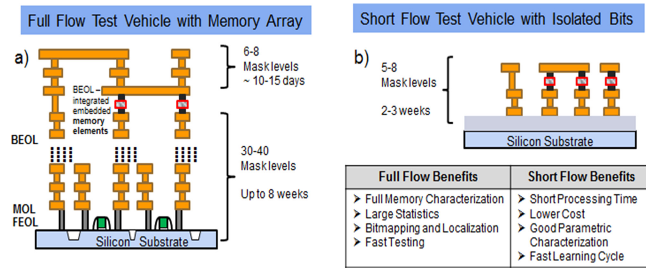
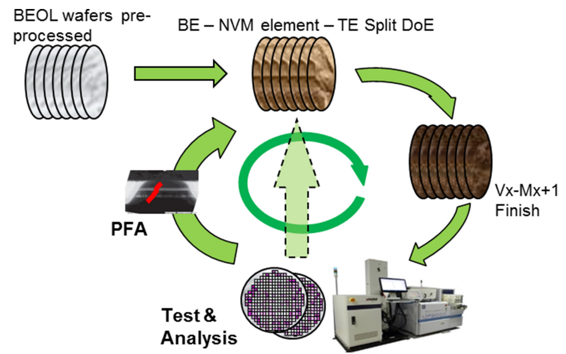


Full Flow Benefits	Short Flow Benefits
➤ Full Memory Characterization ➤ Large Statistics ➤ Bitmapping and Localization ➤ Fast Testing	➤ Short Processing Time ➤ Lower Cost ➤ Good Parametric Characterization ➤ Fast Learning Cycle

FIGURE 1. Comparison of processing complexity between (a) – Full Flow test chip for BEOL-embedded memory and (b) Short Flow test chip. The table shows difference between benefits for each of them.



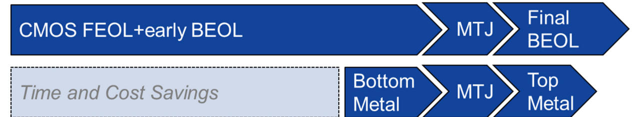


FIGURE 2. Short Flow test vehicle for memory element test enables faster learning cycle and lowers the development cost compared to full flow wafers with integrated memory process. Bottom graph shows potential time saving and impact on learning cycle of embedded memory using Short Flow approach.

optimization, module integration, process adjustments, and co-integration with logic blocks.

In a typical process development workflow, the initial integration work focuses on patterning and layer stacking constructional tasks which can be performed at module level, with short flow validation using planar imaging, cross-sectional analysis and metrology. More advanced characterization requires wafers for electrical measurements. Wafers used for single Bit Cell characterization can be processed as a short flow, with test structures providing direct connectivity to selected bits in array structure [5]. Those tests enable early memory characterization and coarse optimization of the materials, unit process steps, thermal cycles, etc. This approach, however, provides only very limited statistics of bit performance, yield and reliability (Fig. 1).

To gain more insight into the memory yield and systematics, fully testable memory arrays are needed. Emerging memories, although integrated between BEOL metal layers, need logic devices as selectors and to support memory periphery and I/O operations. To build fully addressable arrays, the wafers need to be processed through the entire FEOL and MOL (Middle-of-Line) processes, followed by processing of lower metal levels and the embedded memory module. Finally, the upper metal levels are created to connect memory blocks and logic periphery, route the power and provide connectivity to I/O pads. This is a typical practice in technology development, where fully processed wafers are used to test memory cells and addressable memory arrays.

Fully processed wafers provide not only bit cell parametric information, but also failure bit statistic, which is needed to determine bit yield and to build a failure mode pareto. Such information is needed to understand systematics and process window across array, reticle field, and wafer regions. Logic and Memory testers are used to collect the yield and performance data of memory cells and to assess reliability.

In some embedded applications, memory elements are placed at high interconnect levels, even above Metal-5 [6]–[7]. Processing the wafers through FEOL, MOL, and multiple metal levels significantly increases processing time and wafer cost during technology development and ramp. For that reason, development teams often use short flow processing to build only a subset of the integrated flow, containing only the layers associated with the memory elements. The short flow is used to optimize some of the process steps, even long after the main integration project has been completed. Such approach, however, rarely provides any parametric electrical data.

B. MEMORY CHARACTERIZATION WITH SHORT FLOW TEST STRUCTURES

As mentioned earlier, complete characterization of the memory cells requires a full memory array of desired size and logic-based periphery for Row/Column selection, read circuitry, etc. The memory testing involves writing various patterns to understand cell interaction, detect failure modes and possible spatial signals, caused by cell placements, Row or Column interaction, and possible disturbs during Program, Erase or Read operation. Fully processed arrays are needed also for endurance and data retention reliability tests.

A test chip which can be run and tested in a short flow mode is an attractive alternative. Although not fully functional, it can provide detailed information about memory element performance, yield, and fundamental reliability properties while also being a less expensive, faster learning tool. Benefits of the faster learning cycle are illustrated in Fig. 2. Short flow solutions have been previously proposed to screen materials and collect basic electrical parameters [5]. While useful to support initial development, data volume is limited by the test element count and the throughput of the parametric tester. In addition, the resulting test data statistics are usually insufficient to drive technology development, memory cell optimization and process improvement. To make a short flow test vehicle more effective, a rich statistical data collection approach using high density test

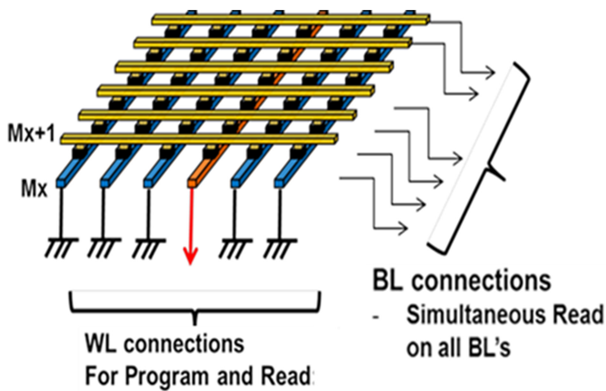


FIGURE 3. Cross Point array of memory elements with simultaneous measurement of multiple elements using parallel test. The memory elements are at the cross-point locations between lower level WL's and upper level BL's.

structures (arrays) is needed. We proposed such an approach to characterize memory elements using short flow test vehicle with cross-point arrays, as shown in Fig. 3 [8]. The arrays can be used to collect data for a large number of bits, check execution of Program/Erase functions, and measure cell resistance in each of the bit states. For efficient testing, this approach requires a flexible, fast, and highly parallel parametric test system for simultaneous probing of multiple structures [9].

There are two consequences of using a short flow and skipping most of the process flow. The first is array connectivity. In order to make they array electrically testable, a special array must be built, using dedicated wiring and with test pad access for electrical wafer probing. The array also must represent real product array layout, with the same cell integration between upper and lower metals, the same cell size, distances, pitches, and placement across the array. Without these constraints, the value of the test data would be rather limited and not representative. The second consequence is limited test coverage. A memory test cannot be used to test cross-point arrays, since there are no Row/Column decoders, so a parametric tester with a pulse generator is typically used. However, it should be noted that the short flow test arrays do not need to be tested in exactly same way as the product arrays to provide feedback useful to process and device engineers. We can define the objective of test arrays in terms of partial memory characterization and set success criteria based on detection of bad bits. For that, the test needs to be able to find and localize bit cells which are either open or shorted, or those which cannot be switched between two logic states, represented by high-resistance state (HRS) and low-resistance state (LRS).

C. TEST CHALLENGES OF PASSIVE CROSS-POINT ARRAYS

To better understand the test challenges, we review the issues related to testing "selectorless" cross-point arrays.

Cross-point architecture of emerging memories with no selectors has long been considered a candidate for high density memories and the problem of "sneak path leakage" and the impact on read margins has been widely discussed in the literature. Researchers from industry [10] and academia [11] applied modeling to tackle design limits of functional arrays, to determine array design and operation margin limitations. These simulation works did not consider practical test or sensing scheme details. Other theoretical studies focused on suppression of sneak path leakage either through circuit design [12] or an intelligent readout scheme [13]–[16]. All of them, however, proposed solutions requiring CMOS periphery accompanying the array, which cannot be used with short flow processed wafers. One study [17] proposed an interesting test approach which used sneak-path current variability to detect memristor array faults. However, this solution required 1T1R cells with transistor selectors to restrict sneak paths to a pre-defined memory region under test.

Experimental work has been presented [18]–[19] that demonstrates RRAM test chip and test system but the solution also needed CMOS FEOL for decoding/multiplexing scheme implemented on silicon. A practical approach for testing RRAM arrays without selectors was proposed in a series of experimental papers in which lab-built microcontroller-based [20], [21] and FPGA-based test systems [22] were used. Their test methods were based on "multi-port readout" [15] and were applicable to short flow arrays. The main drawback of their solution was extensive array test times caused by serial readout of the bits. Another research group developed characterization arrays for wafer scribe-lines, containing an on-chip embedded pulse generator and testable with standard ATE testers [23]. However the solution is not practical for our goals due to the full flow CMOS fabrication requirement.

To summarize, while there have been many ideas proposed to operate a cross-point memory array with no selector and achieving good write/read margins, no working solution has been found. Most existing memory implementations still use selectors either in the FEOL (transistor, diode), or in the BEOL (a nonlinear switch combined with a memory element stack). Similarly, there have been many approaches published to test memory elements on short flow wafers, but test throughput and accuracy limit their applicability to single devices or small 1-D arrays.

Our work follows an approach similar to [21] for "selectorless" cross-point arrays accessed on the wafer with a large multi-pin probe card. We implemented sneak path leakage suppression by grounding unselected WL's and BL's, as proposed earlier in [24] and aligned with [12]–[14]. We also adopted a more extended version of "multiport readout," measuring the current on all array terminals, to calculate and eliminate the contribution of parasitic sneak path leakage.

The array sneak path problem is illustrated in Fig. 4 (a schematic representation of Fig. 3). Let us consider a resistance test of the specific cell located at the intersection of WordLine WL3 and BitLine BL4, marked by the circle. In a two-terminal configuration, with read voltage ("Signal")

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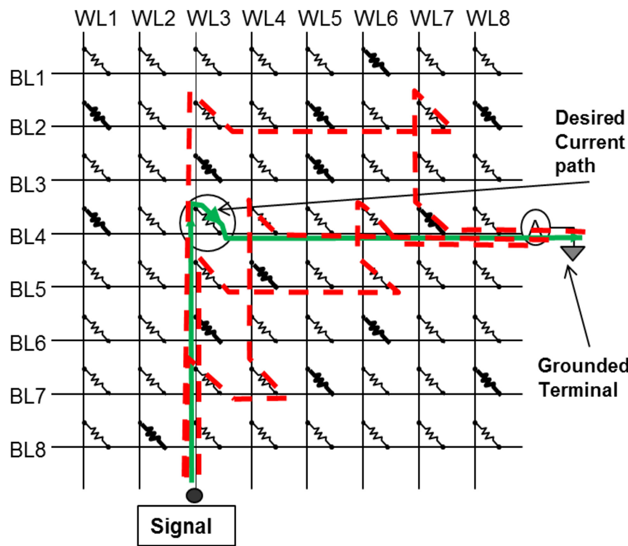

FIGURE 4. Sneaky leakage paths in cross-point array and their impact on resistance measurement of the selected cell. The schematic symbols of the resistors at the crossing of BL's and WL's illustrate cell resistances.

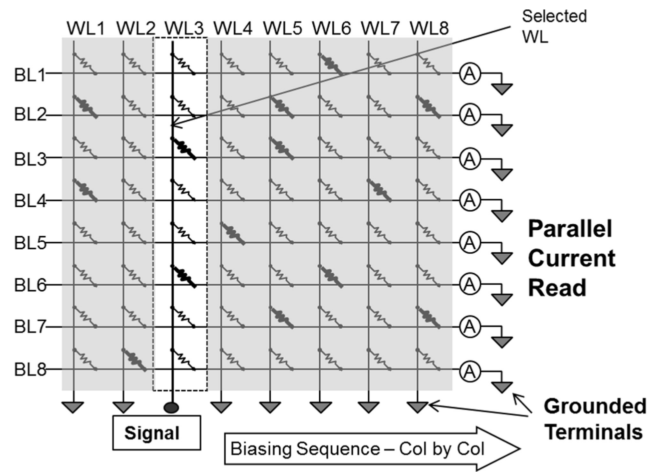

FIGURE 5. Simplified schematics of a cross-point array. During the measurements, all BL and WL terminals, except for Selected WL, are at ground potential.

applied to WL3 and current measured on grounded terminal BL4, the resistance calculated is not just that of a single cell. This is due to additional, "secondary" current paths, illustrated by dashed lines in the figure.

There are many such "secondary" paths and their number increases as the array size increases. These secondary paths are called sneaky leakage paths. Each path is through 3 cells, so the current through a sneaky path is usually much lower than through the selected cell, but the overall effect may be very substantial due to the large number of such paths. Hence the resistance measured between a single selected WL and a single selected BL can be significantly lower than the resistance of the selected cell. An additional selector element has been proposed to block the sneak paths and allow larger array size [10]–[11]. Most embedded memories, however, use a silicon device selector (diode or transistor), which is not readily available in BEOL short flow. Therefore, the proposed arrays need to use a different approach to mitigate the risk of sneaky leakage paths.

Let us consider the ideal cross-point array, with zero-resistance WL's and BL's (i.e., no parasitic resistances), that is tested according to the conditions depicted in Fig. 5. With a single WL3 driving a Read Voltage ("Signal"), all other WL's at ground potential, and all BL's also at ground potential, the only current paths are directly through the selected cells of WL3 and all cell currents are uniquely represented by the currents measured at the BL's terminals. All "secondary" current paths are shut down because the potential differences across all other cells are zero.

Therefore, with the array as in Fig. 5 and with proper test setup (multi-channel parallel tester and pulse generator), it should be possible to measure initial resistance of all the cells, and check if they are fully functional. To achieve this goal, all cells of the array can be programmed into one state, tested for resistances of all elements, then programmed into another state and tested for their resistances again. Since the resistance of each cell can be tested independently, the array can provide valid, bit level information about cell functionality. The statistical size of the data population will depend on the size of the array, and the number of the arrays tested, either in series or in parallel. Therefore, the benefits from building larger cross-point arrays are obvious: (i) more cells can be placed in a single test structure using a similar number of probing pads; (ii) test time per cell can be decreased by testing a larger number of cells on the same WL; and (iii) a larger number of test arrays that can be placed per die, resulting in higher overall fail rate observability per die and per wafer.

There are, however, significant drawbacks when increasing the array size. As mentioned earlier, Fig. 5 is an ideal case. In reality, the cross-point array of cells sandwiched between two conductor layers has many parasitic resistances, some of them localized, and others distributed. Because of these parasitic resistances, the assumption about zero potential difference across all unselected cells is not valid [25].

With increasing distributed resistance between the cells along WordLine and along BitLine, the problem becomes significant, impacting measurement accuracy and ability to detect the resistive state of the cell (especially for low resistive memories, like MRAM). Moreover, increased array size, having more WL and BL connections, requires more probing pads, thus increasing distances and resistances between the array and pad contacts to the tester. Voltage drop along these external array connections causes additional uncertainties and measurement errors.

Fig. 6 shows a schematic of the equivalent circuit of the array including parasitic resistances in the design of the test structure. Clearly, the I_{BL} current measured at each of BL terminals is not just a function of the V_{on} voltage and Cell resistance, but many other parameters.

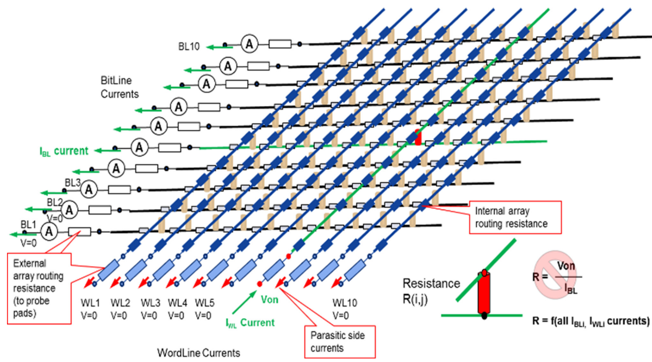

FIGURE 6. **Schematics of a cross-point array with internal and external parasitic resistances. BL/WL current meters represent parametric test (with multi-channel tester). The lower-right corner insert shows the resistance of the selected Cell – this resistance cannot be simply calculated from V_{on} applied to the WL and resulting BL current I_{BL}.**

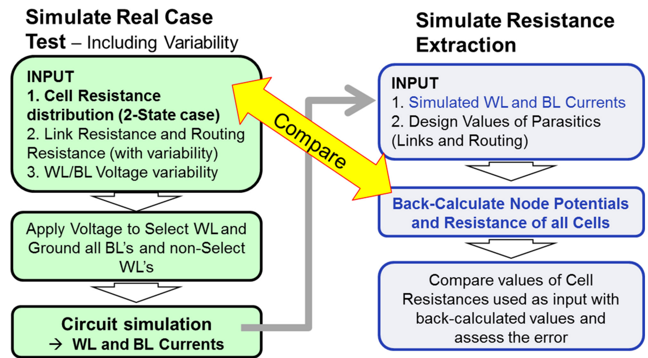

FIGURE 7. **Simulation flow to estimate cell resistance extraction errors.**

Another factor which needs considering for the selectorless cross-point array is a potential risks of voltage overshoot or current spike during the programming pulse, caused by fast resistance change from HRS → LRS (despite wide amount of studies, reviewed earlier in this Section, not much discussion was devoted to this issue). When the parasitic capacitances of the test structure and test system are significant, a sudden resistance drop can cause instantaneous reversal of voltage polarity, causing a discharge and current spike across the unprotected cell.

From our early experiments with PCRAM arrays, which had large resistance change (around 1000 times), we found that they were well protected by internal "load resistance" of the high-resistive heater, and did not show damage. MRAM cell resistance change is only 2-3 times; therefore we do not expect issues related to voltage drop change and overshoot.

As an additional protection, at design level, a protective "load" resistor can be implemented at a WL column level. This extra resistance can be accounted for as part of "extrinsic resistance", further discussed in next Section.

III. CROSS-POINT ARRAY TEST SIMULATION

A. ARRAY MODELING FOR CELL RESISTANCE EXTRACTION

As discussed above, internal and external array parasitic resistances contribute errors when estimating the resistance of array elements. The parasitic resistances are shown in Fig. 6 along with the test conditions and currents measured on array terminals. Typically, only the BL currents are measured to calculate cell resistances. However, in order to estimate the errors, we propose to measure the currents on all WL's as well.

The problem becomes easier to solve when the values of parasitic resistances, or at least their estimates, are known. Using the values of the currents measured on all array terminals, and estimates of the parasitic resistances (from the design), we can solve circuit equations to estimate all node potentials and all internal currents flowing between the nodes.

In the current work, we focus on test simulation, analysis and design optimization of cross-point arrays without selectors. To support this study, we built a circuit simulator which first generates parametrized distributions of array cell resistances and then simulates the test results taking into account all parasitic resistances and their variability.

Both internal and external resistances are design dependent, can vary across a wide range and are difficult to minimize. Precise estimates of their values enable cell resistance extraction with reasonable precision. Hence, using circuit modeling in combination with all-terminal current measurement data, we minimize errors caused by sneaky leakage paths. The solver calculations can be added to the test program and the "back calculation" algorithm can be used for cell resistance extraction during or after the test.

Considering the objective of using a passive cross-point array to test emerging memory cells, we should ensure that the proposed approach can test and extract the following:

- Initial resistance of the memory cells
- Cell resistance after Program and Erase operation (or SET and RESET)
- Identify and localize bad bits – the cells which cannot be programmed or erased ("stuck" at LRS or HRS), or the cells with low HRS/LRS resistance ratio

To estimate the impact of all sources of errors we used circuit simulation to simulate a typical wafer test flow on a given array design and a custom "inverse circuit solver" (or "back-calculation" algorithm) to estimate the array bit cell resistances from the simulated test data. The simulation flow is illustrated in Fig. 7 and is summarized as follows:

1) Generate a random distribution of cell resistances across the array (in most cases a 10 × 10 array) targeted for a given type of memory bit cell (MRAM vs. PCRAM).
2) Generate a random distribution of parasitic link resistances and external resistances around nominal design targets as well as random set of tester channel offsets for forced voltage values.
3) Perform "forward" circuit simulation of the typical wafer test method: a) ground all WL's and BL's, b) apply a voltage bias sequentially to every WL

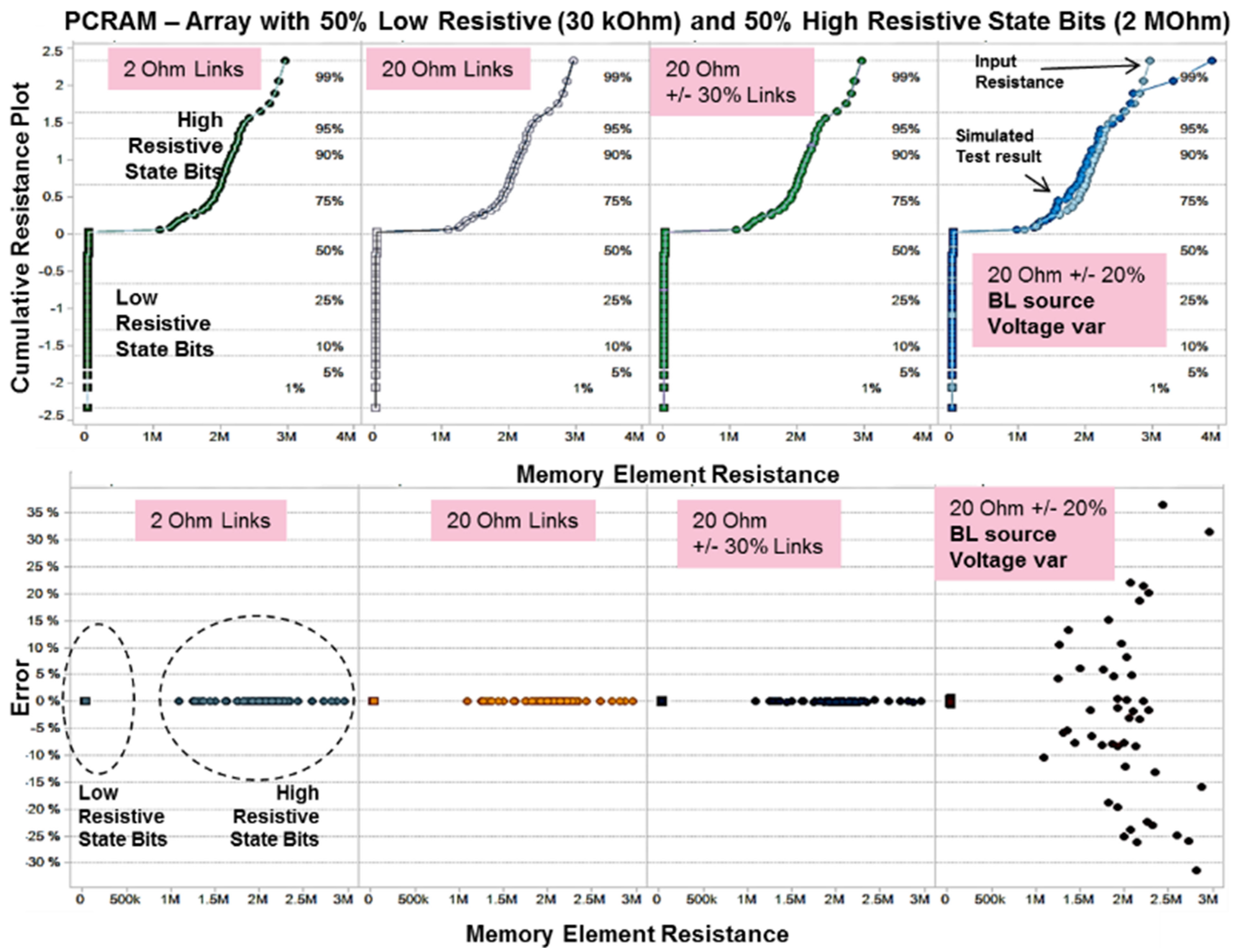

FIGURE 8. Test result simulation for PCRAM Cross Point array with Set (30 kΩ) and Reset (2 MΩ) Bits. Upper plots show Input resistance values and their back-calculated counterparts, and the lower panel show the errors in estimation of resistances. Four panels represent various array design and test conditions.

("walking one"), and, c) for each bias condition, calculate a set of current values for BL's and WL's.

4) Run the simulated BL and WL currents through an "inverse circuit solver" to estimate (or "extract") all cell resistances in the array. For simplicity, the inverse solver assumes nominal values for all parasitic elements and no tester voltage offsets.
5) Finally, the "extracted" cell resistances obtained by the "back-calculation" approach are then compared with "actual" values originally used in the forward simulation and errors were calculated.

While a commercial simulator could have been used for the "forward" simulation, we found it advantageous to develop our own simulation framework using a typical SPICE-like approach [27]. First, the inverse circuit solver needed a fast "forward-solver" in the inner loop. Second, the availability of a compact inverse circuit solver enables "live deployment" on the parametric parallel tester for accurate cell resistance estimation on-the-fly during dynamic test decision-making (e.g., incremental voltage sweeps to drive bits into LRS and HRS states).

All simulations discussed here are of simple DC resistor arrays. However, the simulator also supports dynamic bit-flipping behavior during the simulated test vector sequences (i.e., the "walking one"). Such simulation results are beyond the scope of the present discussion and a subject for future publications.

B. IMPACT OF DESIGN PARAMETERS AND PARASITIC RESISTANCE

As discussed in Section II, minimizing parasitic resistances helps to reduce sneaky leakage paths. Further improvement in the precision of estimated cell resistances then comes from test and circuit simulation. We make several assumptions about the array design and test [26]:

1) in order to reduce voltage drop along the current paths, we assume that the array is designed with low "link" resistance between neighbor bits, both along WL as well as BL (called later "Link R").
2) the resistance of wiring from the access pads to the array BL and WL terminals is minimized and equalized ("External R").

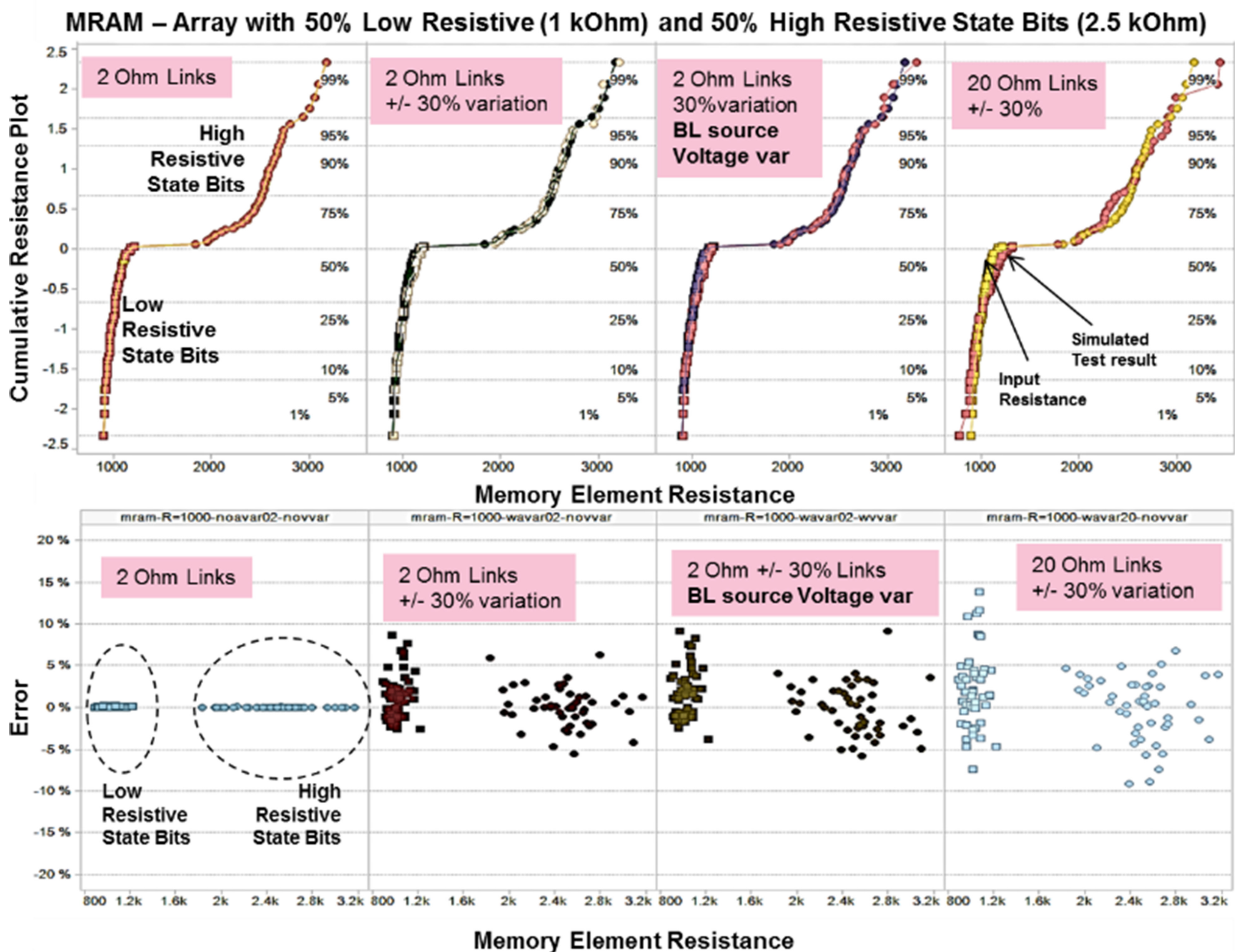

FIGURE 9. Test result simulation for MRAM Cross Point array with Low Resistive (1 kΩ) and High Resistive (2.5 kΩ) Bits. For such low resistance memory cell test the Link resistance introduces additional error of 20-30% (especially when the resistance has high unaccounted for variability). The effect of BL ground potential offset is negligible.

3) a parallel parametric tester is used to simultaneously measure the currents on all BL's and WL's (this is a significant differentiator and method enabler; in a real memory, circuit sense amplifiers are used to detect High/Low resistance state of the cell).

In addition to parasitic resistance we also need to account for current and voltage measurement errors caused by tester channel mismatch.

We performed circuit simulation for two types of emerging memories with distinctive resistance ranges. For MRAM memory cells we assumed 1 kΩ for LRS and 2.5 kΩ for HRS (based on assumptions of MTJ CD $\sim$ 80nm, RA $\sim$ 5 $\Omega.\mu m^2$, and TMR $\sim$ 150% [28], [29]). Respective values for PCRAM of 30 kΩ for LRS and 2 MΩ for HRS were assumed based on [30]. For each case, the resistance distributions were randomly generated for high and low resistance state, and cross-point arrays of 10×10 elements were built. The array design is assumed to minimize internal WL/BL "link resistances" and to check their impact we assumed two cases: 2 Ω and 20 Ω.

The results are shown in Fig. 8 and Fig. 9. The estimates are quite good when the Link resistance has no variability. For the nominal case with no variability, the extracted cell resistance values from back-calculation were found to be essentially identical to their actual values, even for 20 Ω array Bit-to-Bit "link R" connections (see the case of PCRAM in Fig. 8). Additional variability introduces an extra error. For high resistance PCRAM, the error is relatively low: below 1% even with highly variable (30%) link resistance. However, the same link resistance variability can introduce 5-10% error in estimating cell resistance in low resistive memories such as MRAM (Fig. 9). The test results are also sensitive to stability and magnitude of the offset voltage of the BL ground source, which can drive the error to 20% and above, especially for high resistance memories (see Fig. 8 for PCRAM). The reason for such high sensitivity to the offset is the background leakage currents flowing from neighbor BL terminals (in the presence of low resistive cells) into the select BL terminal associated with the high resistance cell.

C. BAD BIT CELL DETECTION

The main application of the cross-point array test structure is to detect bad bits which cannot be toggled between Low-Resistive and High-Resistive states. This capability is absolutely necessary, since quite often bad bits cannot be identified just based on initial cell resistance. As an example we can consider high resistive ReRAM or PCRAM cell which cannot be classified as bad until it fails the Forming operation and programming to a Low-Resistive state. Consequently, one of requirements for cross-point arrays is the capability to distinguish between the LRS and HRS.

A "bad bit" may also be a bit which is permanently shorted and would have much smaller resistance than that expected according to the specification and typical distribution of bits in Low-Resistance state. This could be caused by a sidewall metallic short or bit leakage fault. On the other hand, a "bad bit" may be completely open, with resistance much higher than that expected from the specification for High-Resistance state, and a clear outlier. This might be caused by an open connection to either the upper or lower electrode. Such cells can be easily identified based on the initial resistance estimates, since they are usually more than 6σ from the median of the main distribution and do not respond to Program and Erase operations.

In the following analysis we focus on marginal bad bits - either "stuck at HRS," a bit that does not change its state in response to programming pulses while programming "1," or "stuck at LRS," a bit which does not change under conditions of programming "0."

As found in previous simulation experiments shown in Figs. 8 and 9, the uncertainty and variability of parasitic resistance can significantly impact the accuracy of cell resistance estimation. To demonstrate robustness of cross-point array test, even in the presence of parasitic resistances, we performed simulations of arrays programmed to both Low-Resistance and High-Resistance levels. In both cases we simulated the test with one single bit stuck at the opposite state 3σ from the median nominal resistance. We chose MRAM as an example for this simulation since its low resistance cell is more sensitive to parasitic resistances and sneaky leakage paths in the array.

Fig. 10 shows two plots corresponding to the two "stuck at" situations. Each of the graphs has three panels with the results of simulation according to flow in Fig. 7:

- The first panel shows simulated test data for main LRS or HRS distributions (Fig. 10a or 10b, respectively) with one outlier stuck at opposite state. The outlier is in the tail 3σ away from the median value and close to the main distribution of good bits. The simulation assumes that all design parameters for Link R and External R are known and have no variability. As expected, the bad bit resistance can be extracted very precisely, with no error
- The second panel shows the effect of increasing uncertainty of parasitic link R or/and external R, when the actual values of these parasitic resistances in the array differ 20-50% from the values estimated during design
- The third panel shows the effect of additional random variability +/−15% as is often present in real process. As expected, this unaccounted-for resistance variability causes shifts and widens the distributions.

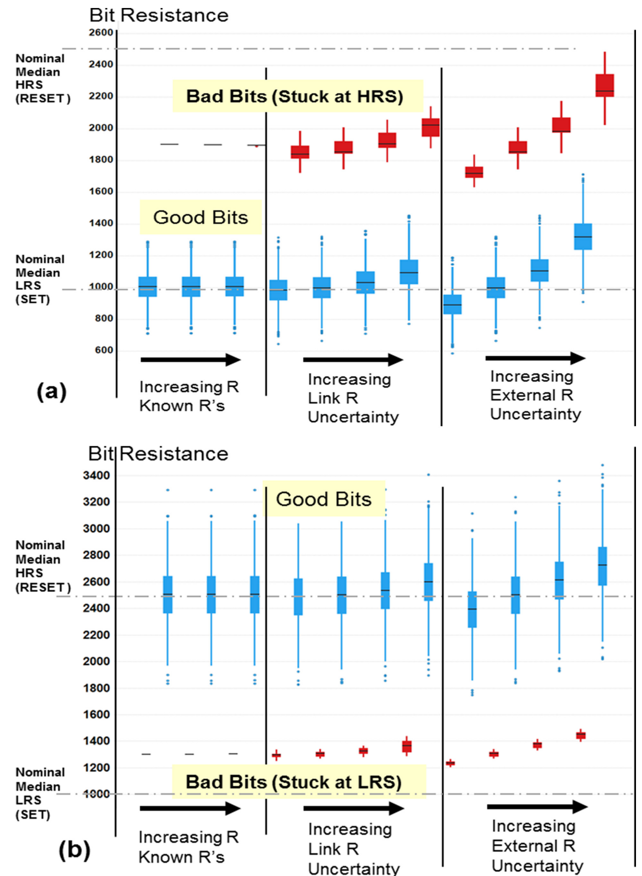

FIGURE 10. Impact of uncertainty in Link Resistance and External Access Resistance values on extracted cell resistance for: (a) Error Bit stuck at High-Resistive State and (b) Error Bit stuck at Low-Resistive State. The distributions of the resistance of single bad bit in the array of 100 bit cells are based on 10 simulation points.

From the results in Fig. 10 we can see that the resistance of "stuck at" bad bits can accurately be identified and distinguished from the main distribution programmed into the opposite state. This is especially true for bad "stuck at LHR" bits, where the impact of parasitic resistances and their uncertainty is much smaller than in case of "stuck at HRS" bits.

D. IMPACT OF ARRAY SIZE

Earlier discussion pointed to the impact of array size on the accuracy of cell resistance estimation. To estimate the impact, we performed additional simulations of cross-point MRAM cell arrays with nominal LRS resistance of 1000 Ω and HRS of 2500 Ω. As in previous simulation, we considered bad bits with resistance 3σ below nominal HRS, at 1900 Ω.

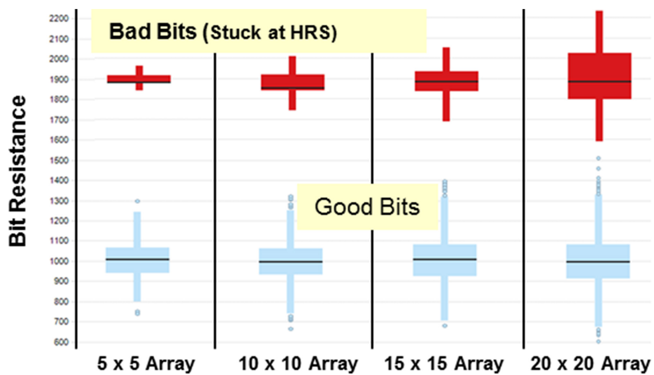

FIGURE 11. Impact of array size on accuracy of bad bit resistance extraction based on multi-terminal current test and back-calculation using nominal parasitic resistance values. Array has unaccounted resistance variability for R Link and for External access resistance at +/ − 15%.

Fig. 11 shows the results of simulated distributions for 10 arrays of various sizes (hence the bad bit distribution includes only 10 points). In the modeled arrays, the resistance of the bad bit is always the same, but the value extracted from test, and corrected using nominal parasitic resistances, varies from case to case. "Stuck at HRS" outlier resistance uncertainty increases with the array size, and in case of the 20×20 array some of the bad bits could be misclassified, as their resistance would overlap with the perceived distribution of resistance of good bits in LRS.

The above results clearly show that the array size needs to be co-optimized with the WL and BL design, depending on bit cell resistance in LRS and HRS. The results also prove that parametric electrical test performed on cross-point arrays, even without selectors, and in presence of sneaky leakage paths, can still distinguish between the cells with high and low resistance state, for both PCRAM and MRAM case.

To summarize, the simulations show that the cross-point array test with post-test correction, using all-terminal current measurements and parasitic resistance models, can be a robust method of identifying bit outliers and bad bits which cannot be flipped from one state into another. Additional design efforts (BL and WL strapping) and test techniques (BL and WL resistance test and BL force voltage zero-offset compensation) can further be used to reduce the test error and provide robust test data for memory bit cell optimization. In addition, array size can also be optimized to provide the best trade-off between the statistical sample size of tested bits, test speed and resistance estimation error.

IV. CONCLUSION

Using extensive simulations, we have demonstrated that cross-point arrays, processed with no selectors, can be used for statistical analysis of the functionality of emerging memory cells. Highly parallel parametric test coupled with optimized cross-point array design offers a good learning tool for a short flow loop characterization. This, in turn, enables a fast and inexpensive approach for process optimization and yield improvement of new emerging memories such as MRAM, ReRAM, or PCRAM.

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